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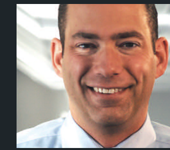

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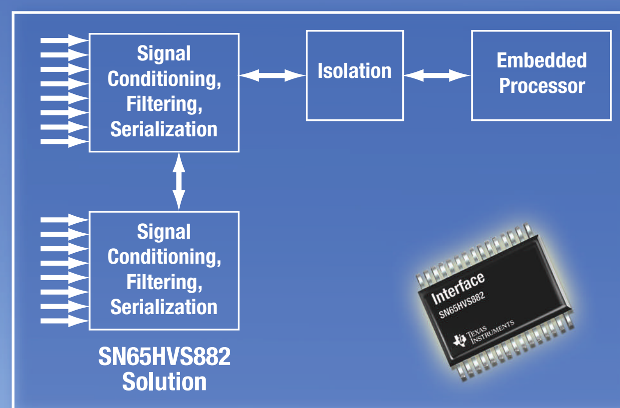

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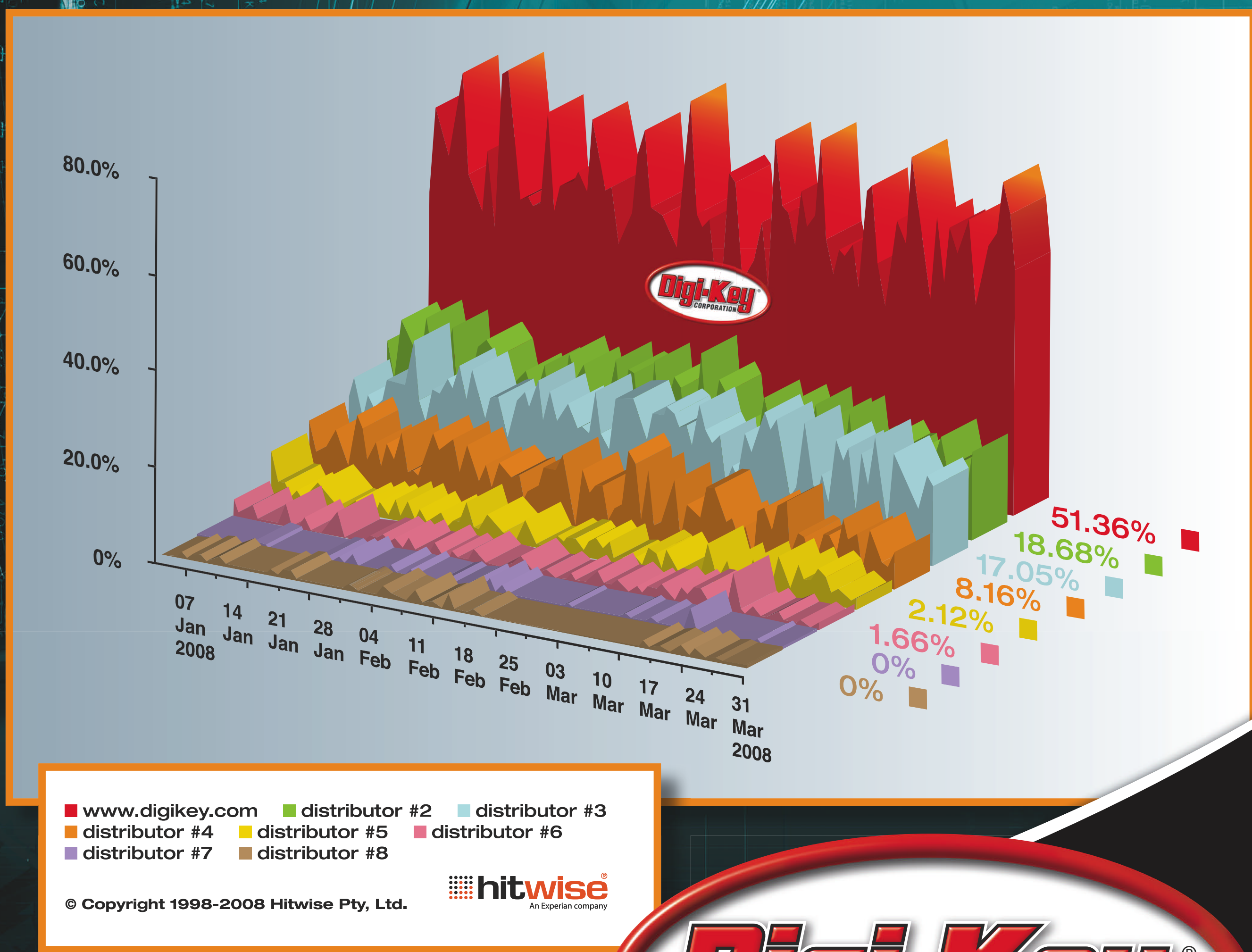

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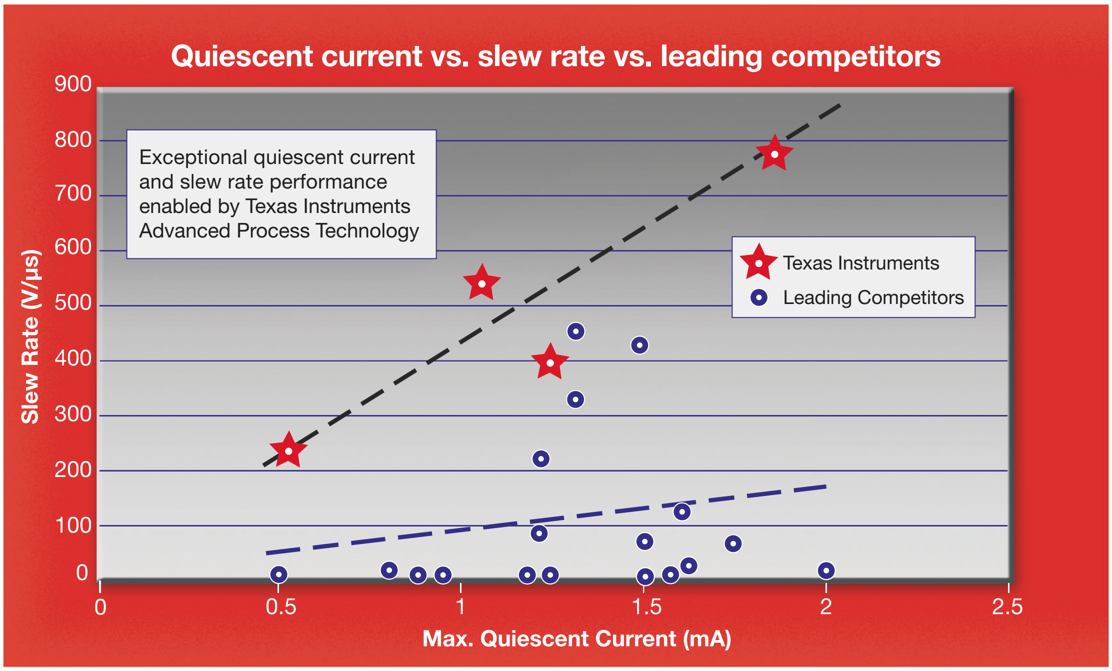

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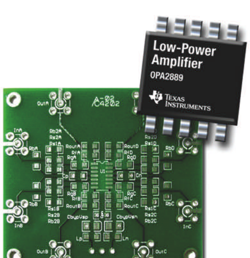

Device	Description
OPA2889	250-V/µs voltage feedback amplifier consumes only 550 µA of I_Q/ch. Device supports 115-MHz bandwidth with supply voltage range of 2.6V to 12V and includes power-down option.
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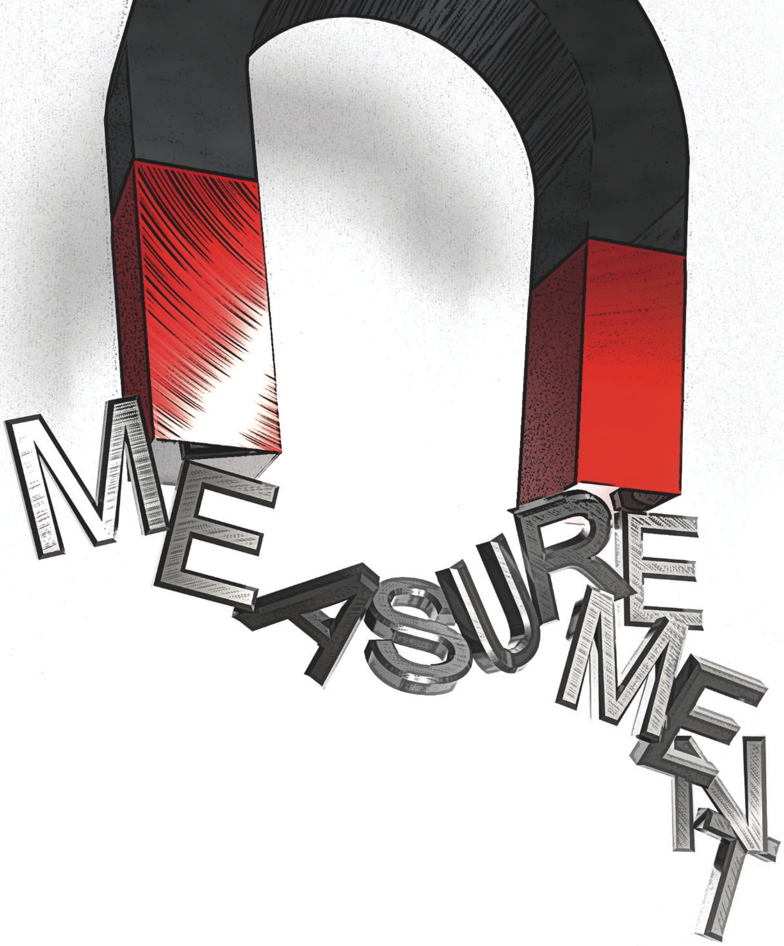

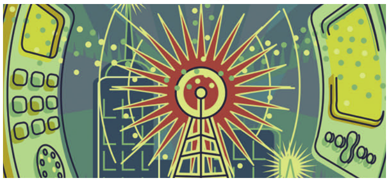

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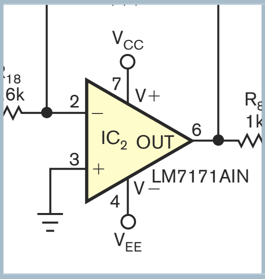

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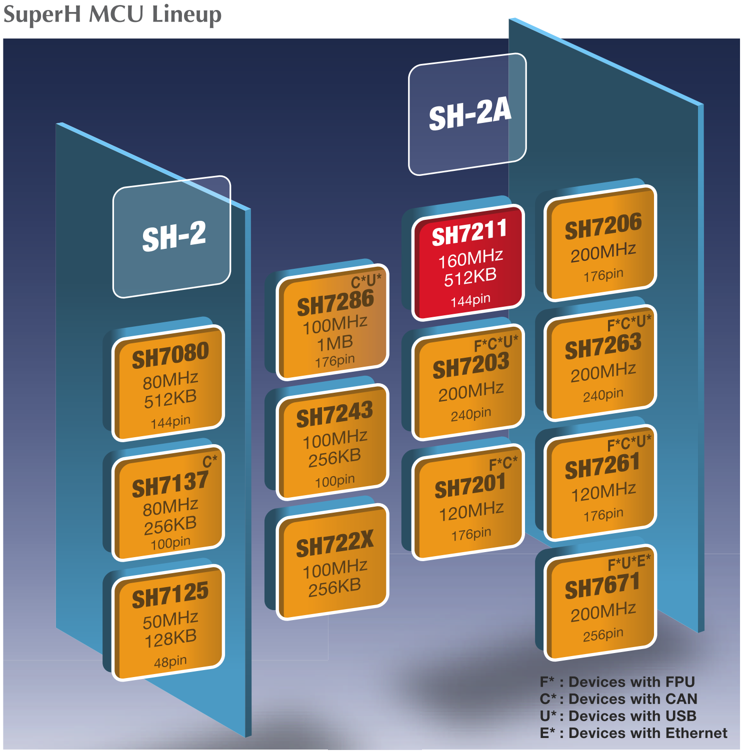
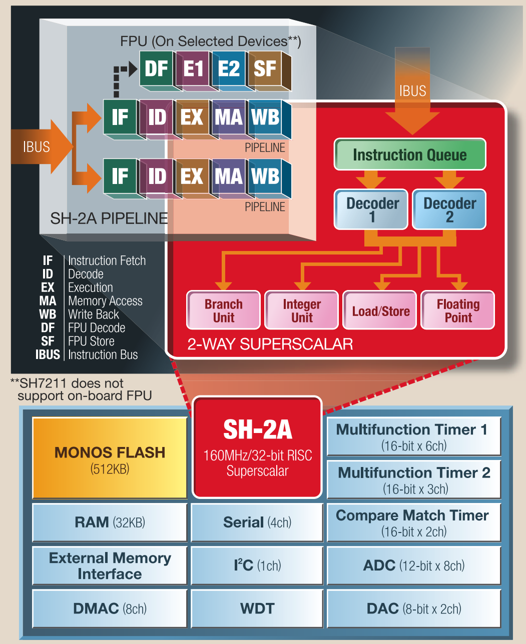


HOT Products | **SH7211F** (R5F72115D160FPV)



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- **High Integration**
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  - Advanced 16-bit PWM timers to drive two motors simultaneously
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*Source: Gartner (March 2007) "2006 Worldwide Microcontroller Vendor Revenue" GJ07168

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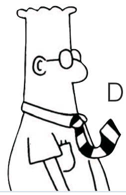

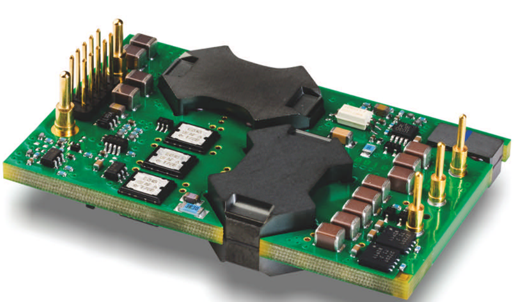

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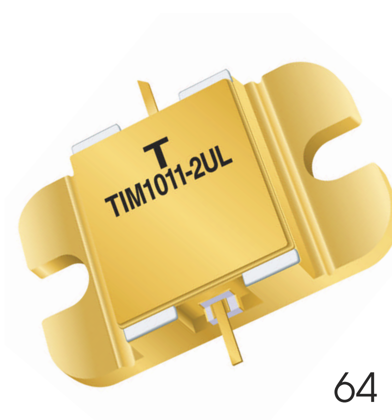

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DEPARTMENTS & COLUMNS

PRODUCT ROUNDUP

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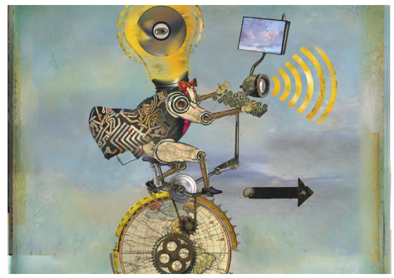

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Innovators 2008: Broadcom's Stephen Palm discusses Wi-Fi and alternative networking technologies.
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EDN.com's quick review of the week in tech.
Tune in on Fridays for "This Week in gEEk," a post in EDN.com's Now Hear This blog that recaps the week's tech news. Catch up on what's happened and get your heads-up on the trends that will be moving the industry in the near future.
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From Embedded Processing, by Robert Cravotta

The experience of a designer moving to embedded-system design.
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BY PAUL RAKO, TECHNICAL EDITOR

The trouble with software people

It started back in 1985. That was when I noticed the trouble with software or, more specifically, the trouble with software engineers. The trouble was that companies were promoting software people with poor programming skills into management. Everyone in Silicon Valley knew that many software engineers getting promotions were the high-dollar folks who could not write good code. The companies they worked for could not easily fire them, so they did what companies often do: They promoted those who lacked programming skills to management. After all, it is a rare breed who can write good, tight code, but anyone can fill out time cards and go to meetings. Unfortunately, those who got promotions were doing more than filling out forms and going to meetings; they were also making product decisions.

In 1985, I was designing an ultraviolet-erasing system for a wafer-probing machine. My boss was a former software engineer. We didn't want the high-voltage-ultraviolet lamp to go on while operators were servicing the machine. We added a key switch to the front panel so a service person could lock out the high voltage. This step required my adding an AND gate to the control circuit.

It was basic: For the lamp to go on, the service person would have to unlock the key switch and the control signal coming from the machine's operating system. But, as I said, my boss had been a software engineer. He didn't like the two-input AND gate that I used for the key-switch function. What if they wanted to change something in the future? So he told me to put in a PAL (programmable-array logic) with eight inputs. In that way, they could have "programmability," he said.

Almost every major development in the last decade has been the result of overcoming the problems that software managers cause.

I tried to convince him of the futility of putting a PAL into a circuit that needed only an AND gate. The other six inputs to the PALs were empty pins, with no other inputs and no other outputs. But the former software engineer knew that programmability was somehow good, especially if it allowed him to weasel out of some previous incompetent decision. He wouldn't relent. I had to put in the PAL, and endure the documentation nightmare of having a programmable device on my board.

The effect of these former software engineers' product decisions is evident everywhere. Rather than have any courage, they make everything configurable, as that former boss of mine tried to do with a PAL. Worse yet, the few times that any sane, normal person might want some configurability, these software bosses fix things in some arcane, absurd procedure that may make sense to unsociable, awkward loners but surely don't make sense to the rest of us. What do you expect from people who count starting at zero?

When you think about it, almost every major development in the last decade has been the result of overcoming the problems that software managers cause. Remember when the software bosses had us dialing up bulletin boards and using the Kermit protocol and an unbelievably complex method for looking at a couple of files on another computer? The Internet was a victory and an obliteration of the geeky, painful, arcane software-boss mentality.

Steve Jobs might have a reputation for being difficult, but he knows software absurdity and has the guts to demand better. A friend told me about Jobs' evaluation of an early version of a backlight for the iPhone. As the backlight dimmed, a perceptible flickering occurred. Software bosses tried to mollify Jobs with the usual software razzmatazz about DACs and square-log gamma curves. Infuriated, he just walked out of the room. The iPhone instead ended up with a control signal with ultrafine steps and smooth dimming. Way to go, Steve. Don't take any guff from those software bosses. **EDN**

Contact me at paul.rako@edn.com.

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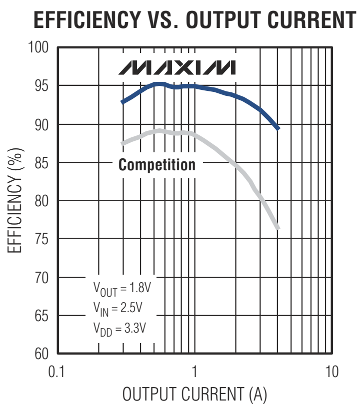

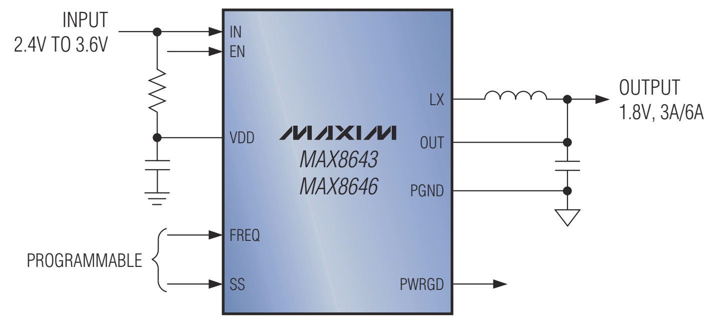

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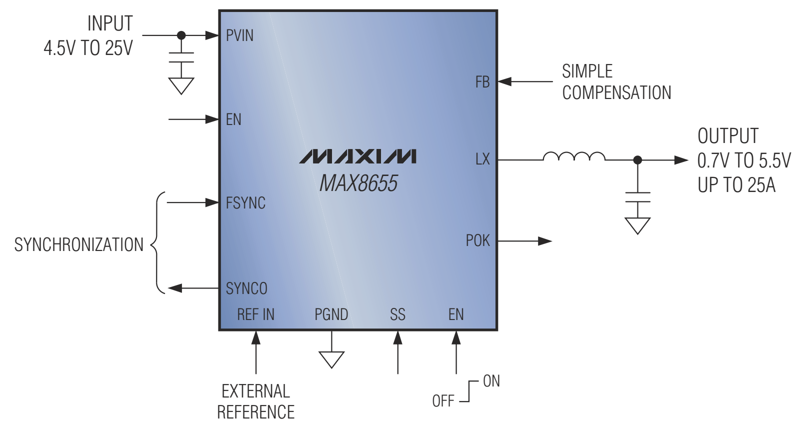

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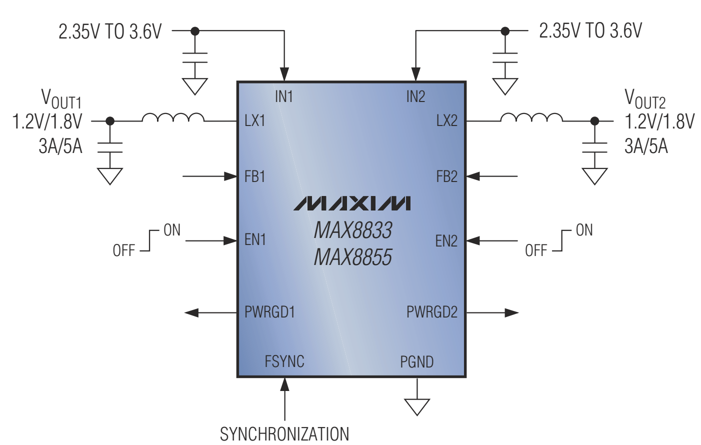

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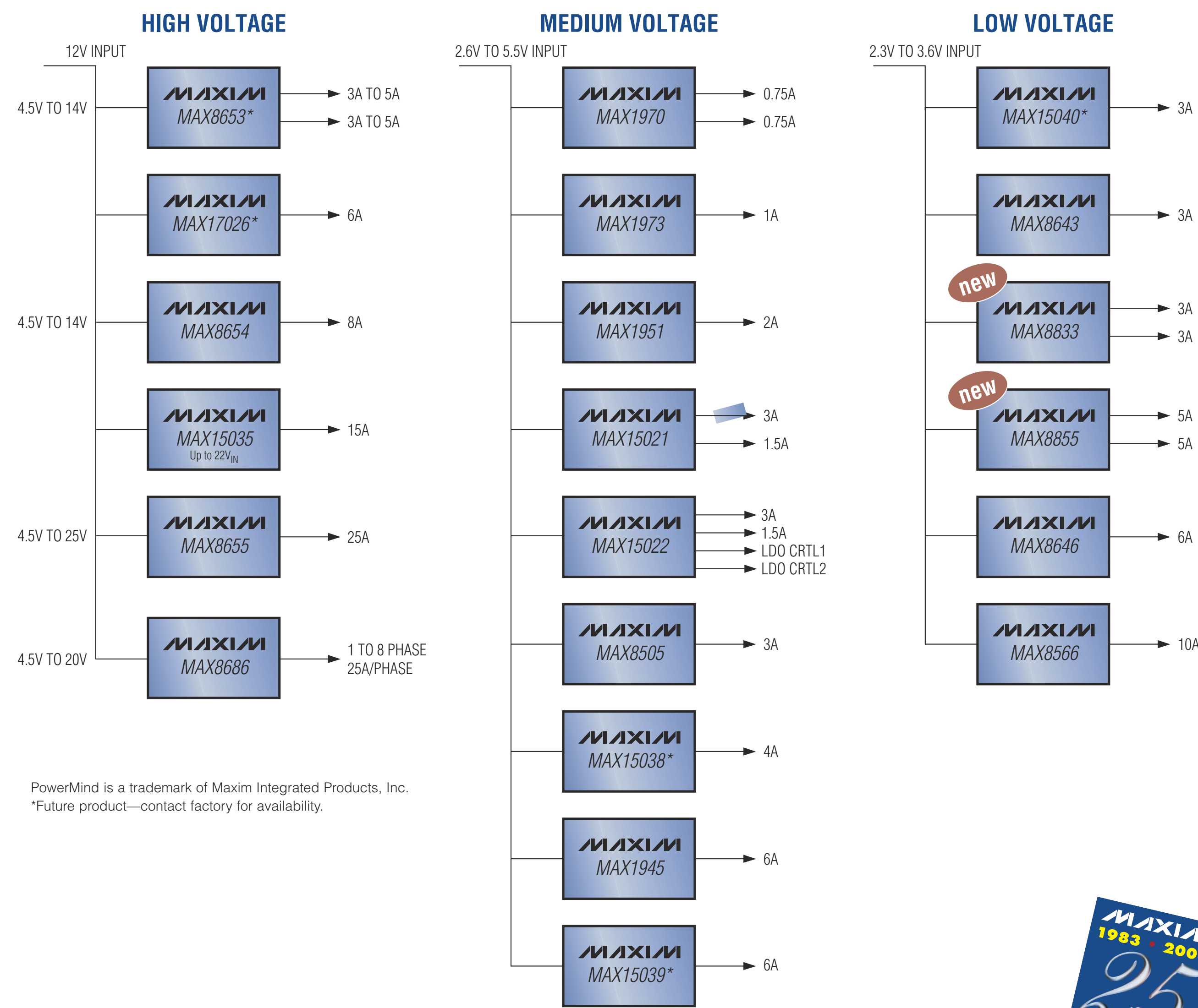

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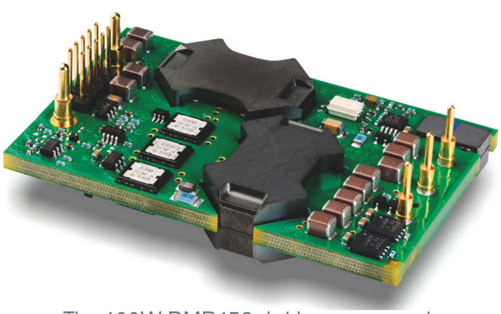
Agilent Technologies

Digital power debuts for 48V-dc servers

Power supplies that rely on analog-control loops may be highly efficient at full load but become less so when the load drops below its tuned "sweet spot." As a result, server farms for the telecom and datacom industries are seeking a digital approach as they grapple with high energy costs because digitally controlled power supplies' savings in energy and maintenance costs quickly outweigh their relatively higher initial costs.



The 400W BMR453 dc/dc-power supply, targeting −40 to −60V-dc datacom/telecom-power supplies, delivers 96% efficiency and ±2% accuracy.

Among the first using a digital-control approach, Ericsson has introduced the BMR453 series of dc/dc converters. Available in quarter-brick, 2.28×1.45-in. modules, they offer as much as 400W output power or 33A with ±2% accuracy and 96% efficiency. The devices rely on a Texas Instruments (www.ti.com) UCD 91XX digital-power controller.

With an input range of 36 to 75V dc and an output range of 9 to 12V, the BMR453 series targets systems that use −48 and −60V nominal input voltages or any system that must use a telecom input voltage with battery backup. The device's wide load regulation also allow its use as an IBC (intermediate-bus controller) in systems with an IBC-powered hard drive that requires a tightly regulated bus voltage.

The BMR453 is available with a PMBus interface for system communication, control, and monitoring or can be hardware-programmed. The BMR453 with a communication interface sells for $55.50 (OEM quantities).

—by Margery Conner

▷**Ericsson**, www.ericsson.com.

FEEDBACK LOOP

"We will have one agency confiscating our light bulbs and another forcing us to spend $10,000 in hazmat fees when we break one of the mandated CFL bulbs. I guess as long as it's for the children …"

—Reader Peter J Merkin, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6531582. Add your comments.

Network processor integrates programmable Ethernet switch

Xelerated's next-generation HX300 network-processor family integrates traffic management and fully programmable Ethernet switches. The Ethernet switches target fiber-access-aggregation switches, GPON (gigabit-passive-optical-network) and EPON (Ethernet-passive-optical-network) line cards, and EADs (Ethernet-access devices).

The HX320 targets CESRs (carrier-Ethernet-switch routers), service routers, legacy systems, 100-Gbps GbE (gigabit Ethernet), 40-Gbps GbE, and OC-768 applications. The HX330 integrates a traffic manager for CESRs, service routers, GPON and EPON line cards, and xDSL (digital-subscriber-line) aggregation. The Xelerated data-flow architecture scales to 100 Gbps full duplex and can support a QOS (quality-of-service)-aware distributed-traffic-management model for either chassis-based switching systems or meshed configurations.

The HX300 family enables fixed-port, stackable, and chassis-based networking systems that you can configure in mesh, ring, star, dual-star, and stackable topologies. The HX300 integrates 100-, 40-, 10-, and 1-GbE ports. It is binary-software-compatible with custom and metropolitan-Ethernet applications for Xelerated's X10 and X11 network-processor families. The HX300 family will be available for sampling in the fourth quarter of 2008. All devices are available in leaded and lead-free packages with options to support industrial-grade temperature.

—by Robert Cravotta

▷**Xelerated**, www.xelerated.com.

Atrenta announces 1Team-Genesis, collaborates with STMicroelectronics

Atrenta Inc announced at the 45th DAC (Design Automation Conference, www.dac.com) the availability of 1Team-Genesis, which focuses on the capture of design specifications, the automated generation of design descriptions and documentation, the rapid exploration of design alternatives, and "correct-by-construction" chip assembly. Ajoy Bose, PhD, chairman, president, and chief executive officer of Atrenta, said at a June 9 DAC press conference that the company's early-design-closure approach allows design capture, verification, optimization, and exploration early in the design flow at the RTL (register-transfer-level) stage, when it's faster and easier to correct problems and explore alternatives.

Bose also said that Atrenta developed the 1Team-Genesis product in part under a strategic collaboration initiative with STMicroelectronics (www.st.com). Philippe Magarshack, vice president for central CAD and design solutions at STMicroelectronics, told press-conference attendees that Atrenta and STMicro have for several years been cooperating on technologies, including DFT (design-for-test) analysis and memory BIST (built-in-self-test) insertion, with the most recent efforts centering on the development of architectural tools to support power, voltage, and clock-domain planning, as well as power-estimation techniques. He noted that collaborative efforts will increasingly move beyond the RTL to address higher-level architectural issues. "We've made Atrenta part of our system-level design flow," he said.

STMicro had been looking for a design environment that could assist at the early stages of the company's SOC (system-on-chip)-product definition and planning, focusing on architectural-level power analysis, estimation, and management and subsequently on top-down timing budgeting, according to Magarshack. He said that the company's R&D partnership with Atrenta would help with the evolution of STMicro's 45- and 32-nm, low-power advanced-design and -process techniques and associated libraries, resulting in better-optimized designs and faster time to market. Atrenta's commitment to EDA standards, such as IPxact, UPF (Unified Power Format), and CPF (Common Power Format), he said, is also key to smoothing implementation and verification.

Atrenta's 1Team platform also includes the previously announced 1Team-Implement product, which facilitates analysis and optimization of physical effects at the RTL. The starting price for 1Team-Genesis is $100,000 for a one-year license.**—by Rick Nelson**

▷**Atrenta**, www.atrenta.com.

CORRECTION: right caption, wrong photo

Our apologies to Pioneer and Sony for a photograph mix-up in our Jan 24, 2008, article "Digital video pushes the embedded-technology envelope." The article reference and caption for Figure 1 describe Sony's full-color OLED (organic-light-emitting-diode) display; however, the photograph shows a flexible passive-matrix OLED that Pioneer Corp developed. The complete article with the correct photos appears at www.edn.com/article/CA6518680. We regret any inconvenience this error may have caused.—by Warren Webb

▷**Sony Corp**, www.sony.com.

▷**Pioneer Corp**, http://pioneer.jp/index-e.html.

DILBERT By Scott Adams

07.24.08

WIRELESS-SENSOR NETWORKS SUPPORT IP TRAFFIC

Jennic has introduced a single-chip implementation for 6LOWPAN (Internet Protocol Version 6 low-power over wireless-personal-area-network) for routing IP (Internet Protocol) traffic over low-power wireless networks. Jennic supplies products in both ZigBee and generic IEEE 802.15.4 wireless areas; this introduction is part of the IEEE 802.15.4 area.

The company says that, in many cases, in industrial and commercial-building networks, the extended-mesh network–as some proponents of ZigBee suggest–may not be the ideal implementation. A more realistic structure for installing wireless-sensor networks in large buildings comprises a local cluster of as many as 70 wirelessly connected nodes, with the clusters connecting to a wired backbone.

Clusters operate on a self-healing tree-type structure. This approach, the company says, fits well with the IP model. Users need not know whether any connection is wired or wireless; they simply address it with the standard tools of the IP environment. Jennic's networking stack runs on its JN5139 32-bit wireless microcontroller and wireless modules.

—by Graham Prophet

▶Jennic, www.jennic.com.

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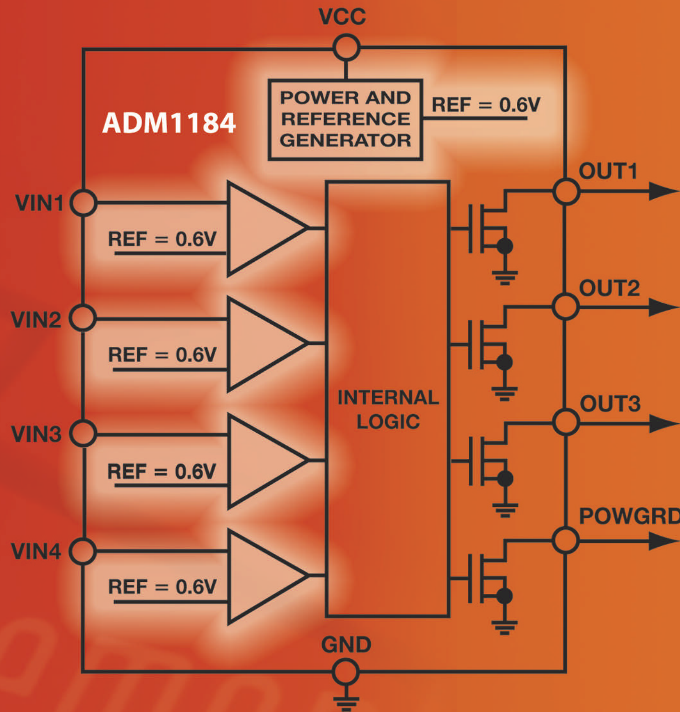

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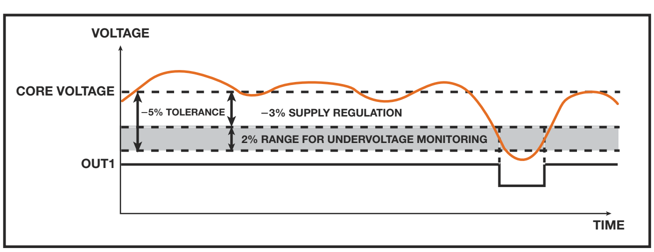

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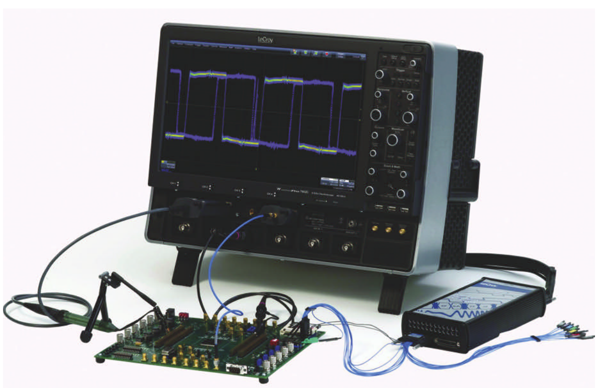
ANALOG DEVICES

New features yield 20-fold speed boost for 1.5- to 6-GHz oscilloscope

It seems as though, almost every month, one of the major digital-oscilloscope manufacturers announces a breakthrough product. Acquisition-memory depth has been increasing: In midrange real-time scopes, LeCroy's newest line offers bandwidths to 6 GHz, four-channel sampling rates to 20G samples/sec, and acquisition-memory options to 128 Mbytes/channel or 256 Mbytes/channel in the two-channel mode, which also doubles the real-time sampling rate.



By adding the module at the lower right, you can turn the WavePro 760Zi into a real-time mixed-signal digital scope with 6 GHz of analog bandwidth, two-channel-mode analog-waveform-capture memory of 256M samples/channel, and waveform-analysis capabilities.

In a related area, the ability to capture long waveform records and to perform complex analyses of acquired data makes painfully obvious any shortcomings in the speed with which a scope processes the data it has acquired. For this reason, all of the major suppliers' recent product introductions have focused on speed improvements in internal data transfers and processing operations. This area, says a LeCroy spokesman, is the one in which the company's newest products, the WavePro 700Zi series scopes and the SDA (serial-data analyzer) 700Zi series, improve on the performance of their predecessors as well as that of their competition by factors that, in some cases, exceed 20. The units derive this speed from the use of quad-core 64-bit processors, a 64-bit operating system, and the new X-Stream II architecture. This improvement is especially dramatic when you equip the new LeCroy units with an optional 8 Gbytes of processor memory. In addition, LeCroy boasts that these new instruments can perform many more analysis functions than can the competition and do so in ways that integrate more gracefully with other scope functions and with third-party analysis packages, such as The MathWorks' (www.mathworks.com) Matlab.

Perhaps the most obvious break with tradition in both of the 700Zi series is the wide-screen display with the soon-to-be-ubiquitous 16-to-9 aspect ratio of digital TV. What's more, the scopes are also just 11.4 in. deep—deeper than the manufacturer's lower-priced units—but occupy much less bench area than most scopes of equivalent bandwidth. All members of both new series provide 1-MΩ and 50Ω inputs and include both BNC and higher-bandwidth input connectors. A LeCroy spokesman acknowledges that, at speeds higher than 3.5 GHz, BNC inputs can introduce unacceptable waveform distortion but notes that most people who buy scopes with bandwidths higher than 3.5 GHz often use the instruments in applications in which the frequencies of interest are lower than 3.5 GHz. It thus makes sense for a scope to be compatible with probes and cables that are abundant in most labs and whose use is acceptable in many applications. The 4- and 6-GHz units also incorporate interfaces to a wide variety of probes.

The key difference between the 700Zi WavePro and SDA series is that the SDA units include twice as much standard waveform memory and incorporate an enhanced high-speed serial-pattern-trigger feature that, on the 4- and 6-GHz units, operates on patterns as long as 80 bits at speeds to 3.125 Gbps. A cable-de-embedding feature removes cable-distortion effects. An IsoBER (bit-error-rate)-analysis feature plots lines of constant BER directly on eye diagrams, enabling designers to understand a receiver's sampling margin directly from the eye diagram and see the direct correlation between sampling margin and BER. The SDA units, which can simultaneously display a data stream's eye diagram, time-interval error, bathtub curve, and jitter histogram, allow users to debug and validate new designs and test compliance with Ethernet, USB, PCIe (peripheral-component-interconnect-express), SATA (serial-advanced-technology-attachment), UWB (ultrawideband), and HDMI (high-definition-multimedia-interface) standards.

Both 700Zi series also include the new TriggerScan exception-triggering feature, which complements the WaveScan feature that LeCroy has offered for several years. WaveScan enables you to automatically search for rare and elusive anomalies in long waveform records even when you can't yet characterize the anomalies. However, the feature works best for finding anomalies in records that you have already captured. TriggerScan requires you to characterize the anomalies before you begin capturing the data, but, once you have done so, it places in memory only those waveforms that meet the trigger criteria. According to LeCroy, TriggerScan gives the scope dramatically less "blind time," the time after each trigger during which it can't capture additional waveforms, than do other ways of finding anomalies. The short blind time enables the scope to find many more anomalous waveforms every minute it spends searching for them. Together, the 700Zi line's scope and SDA series include nine models with bandwidths of 1.5 to 6 GHz. A pair of disk-drive analyzers brings the total number of units to 11. US prices range from $23,500 to $69,400.

—by Dan Strassberg

▷**LeCroy Corp**, www.lecroy.com.


ALTERA
Cyclone III

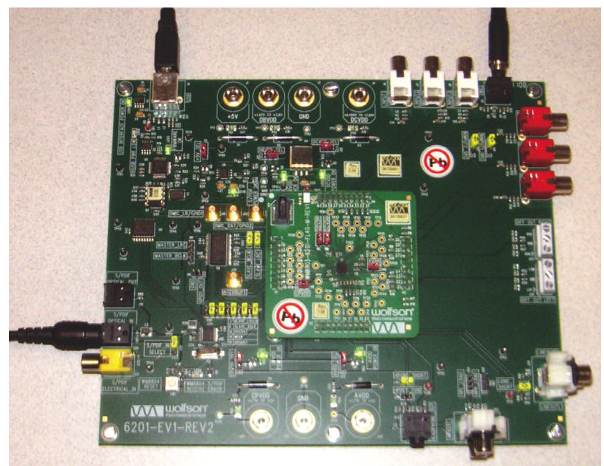
Audio codec incorporates charge pump for Class G headphone amplifier

Wolfson recently announced the low-power WM8903 audio codec for handheld consumer electronics. Wolfson varies the power-supply voltage to the headphone amplifier for Class G operation for a 30% increase in battery life. Furthermore, the DAC employs a capacitor-switching architecture that allows system designers to trade off audio performance for power consumption. Wolfson has also provided an output-clamp circuit that minimizes clicks and pops. The chip integrates a dc servo to control offset voltages through the signal path. The device features a high PSRR (power-supply-rejection ratio) so that you can operate the audio system from a switching power supply. The unit provides a dynamic-range controller that improves the quality and intelligibility of recorded sound. Applications include portable media players, multimedia phones, and digital videocameras.

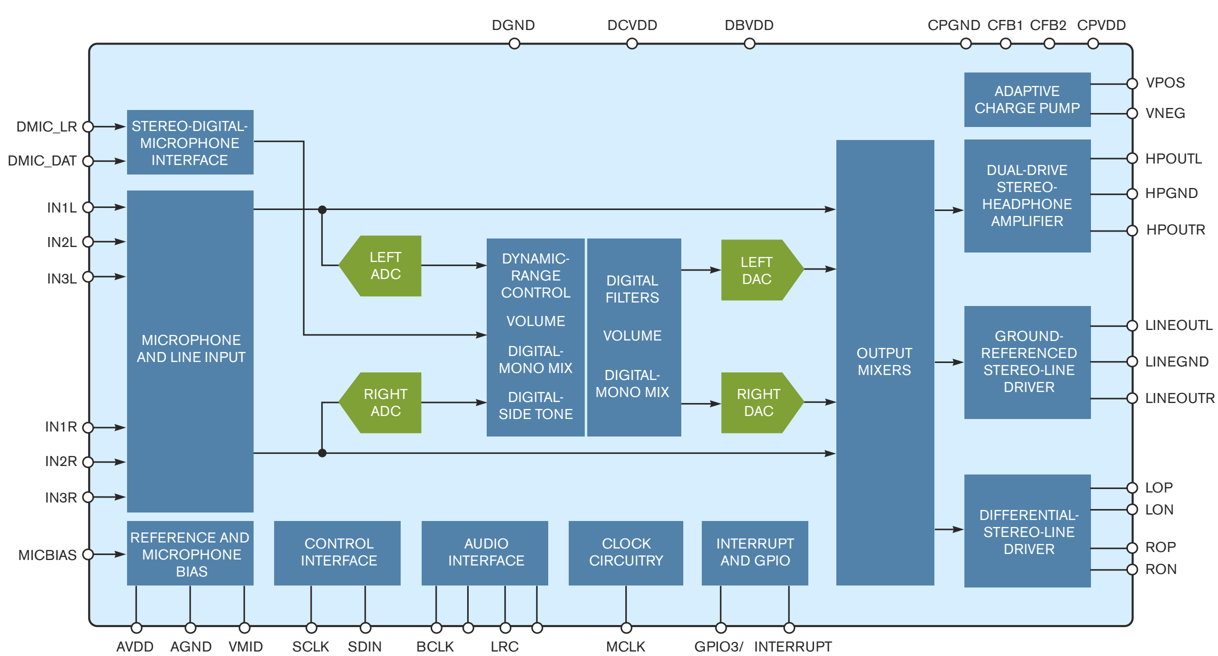
You cannot use headphone amplifiers in a bridge configuration because not all four stereo-speaker leads are available. The stereo plugs tie two of the speaker leads to a common, meaning that single nonbridged amplifiers must drive consumer headphones, thus requiring either an output-coupling capacitor, which allows a single-supply voltage, or a charge pump to create a negative voltage rail. Wolfson uses a charge pump but also modulates the output voltage to lower the power amplifier's supply voltage when the audio is at low volume. The industry refers to this approach as Class G operation, but Wolfson dubs it Class W. To properly evaluate the power savings the chip offers, Wolfson points out, simplistic testing using sine waves does not fully demonstrate the device's real power-saving potential. JEITA (Japan Electronics and Information Technology Industries) tests use a sine wave, but the more sophisticated IEC (International Electrotechnical Commission)-60268-5 test uses filtered pink noise, which better replicates an audio signal and allows system engineers to better explore the true power-saving potential of the chip.

The WM8903 comes in a 40-pin, 5×5×0.55-mm QFN package. The operating-temperature range is −25 to +85°C, and price is $1.80 (10,000). The part is available for sampling now, with production slated for September 2008.**—by Paul Rako**

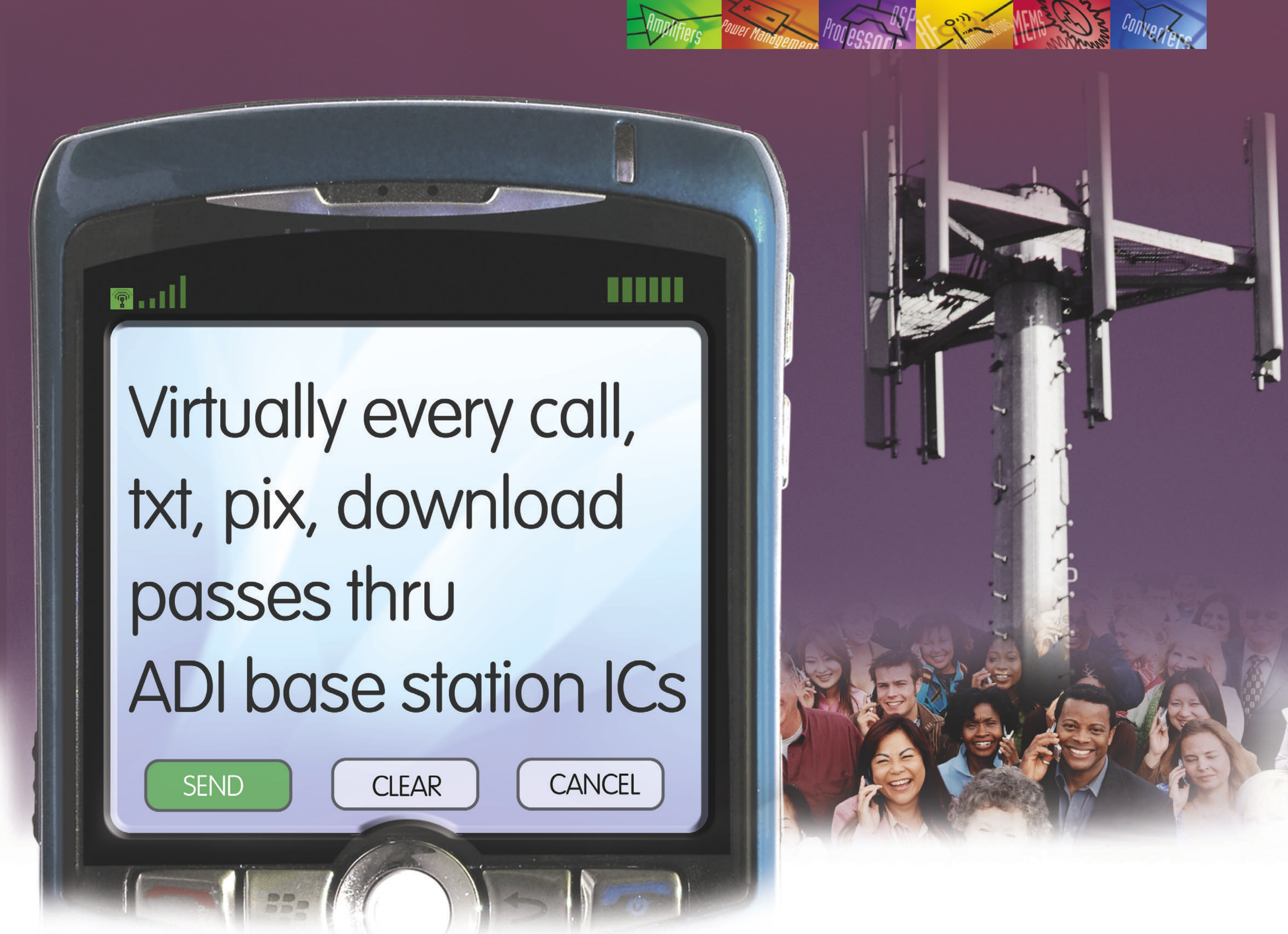
▷**Wolfson Microelectronics**, www.wolfsonmicro.com.



The low-power WM8903 audio codec targets use in handheld consumer electronics.



The Wolfson WM8903 audio codec is available on a demo system with a USB interface.



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ANALOG DEVICES

RESEARCH UPDATE

BY RON WILSON

Inspecting electronic materials—atom by atom

The advantages of imaging individual atoms in electronic materials are obvious. As you learn more about the subtle impact of small quantities of impurities on a crystal, for example, it becomes more important to know just where and in what orientation the impure atoms reside. In principle, this ability should represent the great promise of the electron microscope. The wavelength of electrons is sufficiently short to allow the necessary resolution. But traditional transmission-electron-microscope resolution was only approximately 1 nm—not nearly fine enough. The main limiting factors were not the electrons but two unrelated factors: the stability of the sample stage and the aberrations in the electron optics.

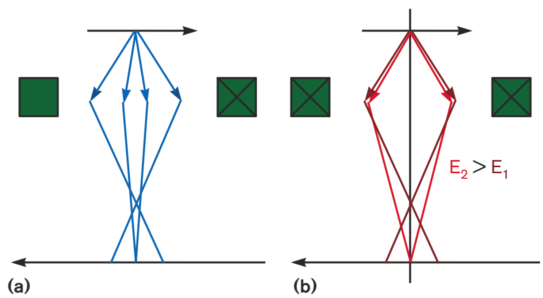
In recent years, a number of research projects, including the TEAM (Transmission Electron Aberration-Corrected Microscope) project at the University of California–Berkeley and a separate project at the Max Planck Institute of Biophysics, have been systematically attacking these limitations. Last month, a paper from the Max Planck Institute at Microscience 2008 in London gave an update on the progress to date. The stability problem, as it turns out, also plagues the developers of atomic-force microscopes, so considerable progress has occurred in this area. Improvement in this stage means simply adopting the mechanics the atomic-force instruments use.

The optics problem is separate. The TEAM project has announced the installation at the Berkeley facility of an instrument with a demonstrated 0.05-nm resolution—which the researchers achieved by correcting for spherical aberration—and researchers will be able to use that instrument by this fall. A follow-on phase of the project will go after chromatic aberration. The Planck Institute appears to have achieved 0.08-nm resolution on its instrument with its own spherical-correction technique.

The results are dramatic: transmission-microscope images of individual atoms within a lattice. As these instruments move from the research lab and into regular use, the results could be remarkable, revising everything you thought you knew about the properties of materials.

▷**University of California–Berkeley**, http://berkeley.edu.

▷**Max Planck Institute of Biophysics**, www.mpibp-frankfurt.mpg.de.



Both spherical (a) and chromatic aberrations (b) degrade resolution in electron microscopes.

CARBON NANOTUBES MAY HAVE A DARKER SIDE

The apparent harmlessness of carbon nanotubes has so far kept them outside the growing debate about the potential hazards of nanotechnology. Scientists believed that the structures were insoluble in water, and they appeared to offer no threat to biological organisms. But that picture seems to be changing. Recent research has suggested that nanotubes may in fact have some solubility in water, and a recent paper in *Nature Nanotechnology* (http://npg.nature.com/nnano/journal/v3/n6/abs/nnano.2008.109.html) suggests that nanotubes clearly interact with certain protozoa. Unfortunately, the protozoa in question are not just laboratory curiosities, but rather organisms that are vital to biological treatment of waste water and possibly necessary for controlling bacteria populations in nature.

Researchers at the University of Waterloo exposed the protozoa tetrahymena thermophila–a rather voracious bacteriophage–to single-walled carbon nanotubes. The organisms exhibited a range of responses, depending on the concentration of nanotubes, varying from reduced mobility to clumping into clusters to dying outright. In most cases, the protozoa ingested the nanotube particles, which was of concern to researchers.

This taste for the unusual suggests that the protozoa could concentrate nanotube fragments from the environment and pass them up the food chain, with completely unknown consequences. Another serious issue is that, in most cases, the protozoa's ability to ingest bacteria decreased after they came in contact with the nanotubes. In, for example, sewage-treatment plants that use tetrahymena, the consequences are obviously negative. But the researchers pointed out that, if nanotube fragments somehow entered a natural environment, the result might be to eliminate a major control on bacterial populations, again with unknown results.

These results do not predict an ecological catastrophe. Rather, as the researchers point out, they turn a spotlight on our near-total ignorance of the interaction between nanoparticles in general and biological systems in general. And they show one instance in which scientists could build a disaster scenario upon an interaction they demonstrated in the lab. Given this data and the absence of almost any other knowledge, it might be just as well to treat nanoparticles as ecologically dangerous and handle them accordingly.

▶University of Waterloo, www.uwaterloo.ca.

07.24.08

BY DOUG SMITH

Crossing the river

Cross a river without a bridge, and your clothes get soaked. Cross a split-plane gap with a high-speed signal, and your whole development schedule gets soaked.

As an EMI (electromagnetic-interference) specialist, I have known for years that a high-speed signal crossing a split or gap in its solid reference plane generates EMI. The first thing I do when troubleshooting a PCB (printed-circuit-board) design is shine a light through the board to look for splits. That trick immediately spots any traces that cross the splits. Of course, I can see only those splits that completely penetrate all the planes in the circuit, but it's surprising how many times this simple check pays off.

A split in the planes causes an impedance discontinuity in the signal path crossing the split. The discontinuity reflects energy back toward the source. It turns out that the split reflects only higher-frequency components of the incoming signal. Removing those components degrades the rise time of the remaining signal that crosses the split.

To demonstrate rise-time degradation, I fabricated a small PCB with two straight traces, each about 15 cm long (**Figure 1**). The board has a signal-ground-power-signal stackup, typical for a four-layer design. Trace A, a 50Ω microstrip configuration, routes on Layer 1 over solid ground metal its whole length in. Trace B uses the same configuration but crosses a break in the planes. The break is a narrow, 5-cm-long gash. The break penetrates both solid reference planes. The auxiliary output of my Agilent Infiniium scope drives the traces one at a time. **Figure 1** superimposes the two results, showing significantly different rise times (300 versus 400 psec). The faster signal is the one over a solid ground plane. If your plane splits exceed 5 cm, expect even more pronounced effects than these ones.

Two explanations for the rise-time degradation come to mind. One is that the split in the planes forms an impedance discontinuity that reflects energy, representing the difference between the two results. Another explanation, possibly oversimplified for this case because of the circuit dimensions, involves lumped-element equivalent circuits. The lumped-element view supposes that signal current flows on Trace B straight across the gap and that an equal but opposite returning signal current flows in the adjacent ground plane. At the break, the returning signal current must pass around the ends of the break to either side of the signal trace. It cannot leap across the gap. The diversion of returning signal current away from the main signal current creates inductance, which filters out higher-frequency components of the incoming signal.

Whichever way you think of it, any significant slowing of your signal rise or fall time can lead to a number of undesirable effects.

Next time you analyze a PCB layout, keep in mind that crossing splits in the planes can cause problems with radiated emissions, immunity to external signals, crosstalk, jitter, and degraded rise and fall times. Don't get soaked by this one! EDN

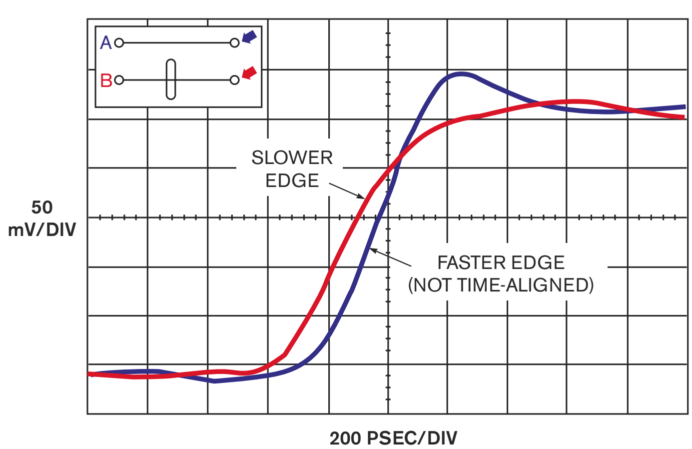


Figure 1 A signal crossing a plane split (red) has a slower rise time than the one with a solid, continuous reference plane (blue) (adapted with permission from http://emcesd.com/tt2005/tt010105.htm).

Doug Smith is an independent consultant specializing in EMI/ESD (electrostatic-discharge) design. Visit his Web site at www.dsmith.org. Howard Johnson will return after a summer break.

www.edn.com/signalintegrity

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National Semiconductor

BY JOSHUA ISRAELSOHN, CONTRIBUTING TECHNICAL EDITOR

The secret, nonspectral lives of analog-input filters

Analog-filter designs manage an uncommonly large number of core parameters compared with designs of other analog-circuit-block types. First, the application usually suggests the overall spectral shape or passband type—lowpass, highpass, bandpass, or band-reject.

Given a shape, the next consideration is usually that of the filter's corner frequency or frequencies. In peak and notch filters, the center frequency and a bandwidth often replace the corner-frequency specifications. Many applications traditionally express bandwidth in terms of Q—a reciprocal measure of bandwidth numerically related to the center frequency.

The parameters thus far describe ideal filters. Real implementations exhibit nonideal traits, some of which specific designs can influence. Examples include nonzero passband ripple and finite transition-band slope. Your application's requirements of these parameters inform the filter's complex-plane geometry, often selecting among, but not necessarily limited to, the classical shapes of Butterworth, Bessel, and Chebyshev. These choices optimize various time- or frequency-domain filter characteristics, including spectral flatness, phase coherence, and transition-band steepness near the corner frequency. Other parameters of concern to some applications include insertion loss and stopband ripple.

Once you've worked through all of these issues, you're on to implementation-circuit topology, component selection, and a brief, heartfelt declaration of victory. Well … that is, as long as your filter feeds a TILC (time-invariant linear circuit)—the kind of circuit to which all of your early circuit-analysis training applies. Alas, in the case of input filters, the next stage is nowadays often a multiplexer or a digitizer—usually an ADC—and these are *not* TILCs.

Your filter design must accommodate its client's input characteristics to minimize the parasitic interactions between the two.

Many ADC ICs provide buffered inputs, which integrate an operational amplifier or a differential amplifier between the input pin or pins and the digitizer circuitry. Multiplexers and unbuffered ADCs, by contrast, bring your source signal directly to a switching input. When using these devices, your filter design must accommodate its client's input characteristics to minimize the parasitic interactions between the two.

These interactions share a common trait: They derive from charge quanta that input-circuit switching devices inject. This charge injection manifests itself as current impulses that reflect in the filter's output impedance and result in an error voltage.

This simplest input filter is a passive-RC arrangement. The charge—the time integral of the current impulse—adds to the charge on the filter's capacitor and creates an error voltage, $dV=dQ/C$, where dQ is the injected charge and C is the capacitance. Assuming a high-impedance input stage, such as a noninverting buffer amplifier following an input multiplexer, the error voltage can decay only by leaking the excess charge into the signal source through the filter's resistance. The charge quantum and the filter capacitance determine the peak-error voltage. The filter's time constant determines the error-voltage-recovery dynamic.

Active filters with RC-output stages, including many filters with odd numbers of poles, behave like passive-RC sections. Active filters with op-amp outputs exhibit a different behavior in which the amplifier's dynamic output impedance determines the peak-error voltage and the amplifier's loop characteristics determine the error-voltage-recovery dynamic.EDN

Joshua Israelsohn is a co-founder of JAS Technical Media, where he manages the company's technical-communication services practice. You can find his contact information at www.jas-technicalmedia.com.

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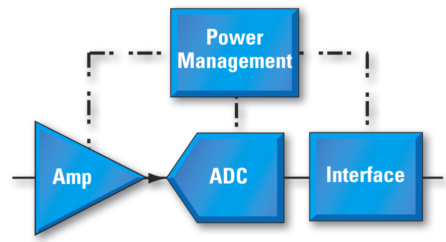

PowerWise Metrics Help Designers Compare Analog Components

PowerWise metrics are formulas and thresholds that distinguish energy efficient components from those that are less efficient. National has developed PowerWise metrics for 24 product categories and selected the best-in-class energy efficient products in each of these categories. Each PowerWise product has a PowerWise label and rating which summarizes its key specifications.

PowerWise® Efficiency Ratings
(4 out of 24 categories shown)

Product Family	Metric	Threshold	Units
Switching Regulators	Peak Efficiency	≥ 95	%
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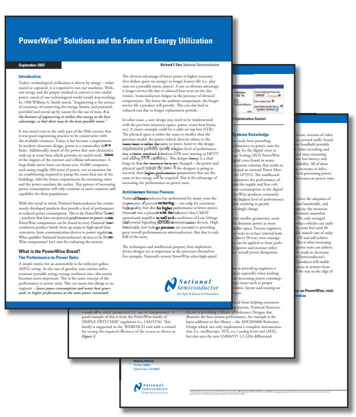

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RAQ's

Rarely Asked Questions

Strange stories from the call logs of Analog Devices

Contributing Writer James Bryant has been a European Applications Manager with Analog Devices since 1982. He holds a degree in Physics and Philosophy from the University of Leeds. He is also C.Eng., Eur.Eng., MIEE, and an FBIS. In addition to his passion for engineering, James is a radio ham and holds the call sign G4CLF.

Stress Is Bad For You — and For Analog ICs

Q. You recently mentioned that mechanical stress alters the calibration of precision analog ICs. Does this mean that mounting them incorrectly can make them inaccurate?

A. Indeed it does! But do not worry too much. We recently discussed the mechanism involved. If a thin film of a conductor is attached to sheet of an insulator its resistance will vary as the insulator is flexed. If the conductor is a resistor in a precision IC stress will affect the circuit's calibration.

This is rarely a serious problem. Precision analog ICs usually rely on the matching of resistors rather than their absolute value. If a chip is laid out so that all its critical resistors experience the same stresses, their matching is maintained even if the absolute values change.

Furthermore if the chip is in a standard IC package its leads (or pads) and bond wires isolate the chip from the small stresses involved in mounting the IC on its circuit board. If a circuit board carrying an accurate analog IC is bent or twisted it is likely that the solder joints will be damaged before the change in accuracy becomes important.

Where problems can and do arise is when ICs are mounted in some sort of mechanical assembly. This is quite commonly done with sensors, which can include temperature sensors, photo-sensors, accelerometers and gyroscopes.

Some engineers feel that these should be mounted "firmly" and this can involve clamping with much higher force than is either necessary or safe. ICs are very small and light, most weigh tens or hundreds of mg and the heaviest are only a few gm. A clamp force of at most one newton[1] is more than adequate to secure them firmly without upsetting their calibration.

I have seen a temperature sensor mounted "firmly for good thermal contact" with a force of some 200 N, which moved the calibration by over 8°C. Experiment showed that the thermal conductivity between the device and the substrate did not change measurably as the mounting force was changed from 1 N to 200 N — but the calibration surely did.

ICs which are mounted in mechanical structures should held with as little force as possible. If they are held in screwed brackets a small piece of foam may be used to limit force but make the mounting more secure. However there should be no foam between a temperature sensor and the surface it is measuring, since this reduces thermal conductivity, nor between a gyro/accelerometer and its mount because it damps HF vibrations.

[1] A newton is more formally defined at http://en.wikipedia.org/wiki/Newton but it is easiest to think of it as the force exerted by Earth's gravity on a small (102 gm) apple.

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PROTOTYPING WITH FPGAs WORKS BEST IF YOU DO IT WITH THE FINAL ASIC IN MIND.

HDL-design challenges and philosophies for real-world ASIC implementations

BY JESSE CHEN • SILVUS TECHNOLOGIES

New requirements for the MAC (medium-access control) and PHY (physical-layer interface) of a wireless-communications system can pose significant challenges for system designers looking to quickly get from development to production. This situation holds especially true as the demands for wireless connectivity and increased data rates continue to grow rapidly. The migration to new standards, such as 802.11n and WiMax (worldwide interoperability for microwave), requires designers to add new features, which necessitates the addition of a significant number of resources to design validation, testing, and integration of already-large, complex designs. FPGAs are excellent, cost-effective resources when it comes to initial design validation. Designers may spend a considerable amount of time prototyping not only new functional blocks, but also the entire wireless system on an FPGA platform.

When a design cycle reaches the point at which a custom-silicon option is necessary for real-world performance and reliability testing, designers must translate the FPGA design into an ASIC implementation for the end product to be viable. This situation ultimately leads to a key question for any SOC (system-on-chip) developer looking to add cutting-edge wireless functions to a design: How can you make the transition from a rock-solid FPGA design to a viable ASIC as swift and as painless as possible? The answer lies in an HDL (hardware-description-language)-design philosophy that keeps in mind from the outset the needs of the ASIC engineers: speed, area, and power efficiency.

FPGAs AND ASICs

Often, wireless-system designers who are developing their prototypes for validation on an FPGA are perfectly content with designs that run at speeds significantly lower than the target application requires. They expect a significant speed increase when porting the FPGA design to an ASIC implementation. This expectation is not unreasonable; users have reported FPGA designs containing logic, memory, and DSP blocks to experience an approximately threefold speed increase when porting them to a standard-cell ASIC of the same technology—that is, the same minimum feature size (**Reference 1**). However, you need not be content with passively

AT A GLANCE

- An HDL (hardware-description-language)-design philosophy must keep in mind the needs of ASIC engineers: speed, area, and power efficiency.
- You need not be content with passively hoping that faster blocks will give you a faster system.
- Any performance increase in the design due to migration from an FPGA to an ASIC directly increases the design-speed margin.
- ASIC designers have turned to multiple-supply and multiple-threshold design techniques.
- "Siliconization"-design and HDL-coding guidelines ensure swift and seamless porting of FPGA designs to ASIC designs.

hoping that faster blocks will give you a faster system. When porting a typical FPGA design, including logic, memory, and DSP blocks, to a standard-cell ASIC of the same technology, one example showed a 20-fold increase in area performance, a twofold to threefold increase in speed, and a ninefold increase in dynamic power.

Both power and speed are critical metrics of a wireless-communications system. Companies often design—and heavily optimize—802.11n PHY and MAC IP (intellectual property) to run on an FPGA at the target speed that the final ASIC implementation requires: clock speeds in excess of 100 MHz for the critical, fastest signal-processing clock domain in the PHY. This optimization benefits both the IP designer and the customer by allowing validation of the design on a real-world platform with real-world situations. When the vendor enables true over-the-air data transmission and interoperability with consumer off-the-shelf hardware, there is no longer a need to rely on the promised, though unknown, performance increase that an ASIC offers. This relief increases confidence in the validity of the design in

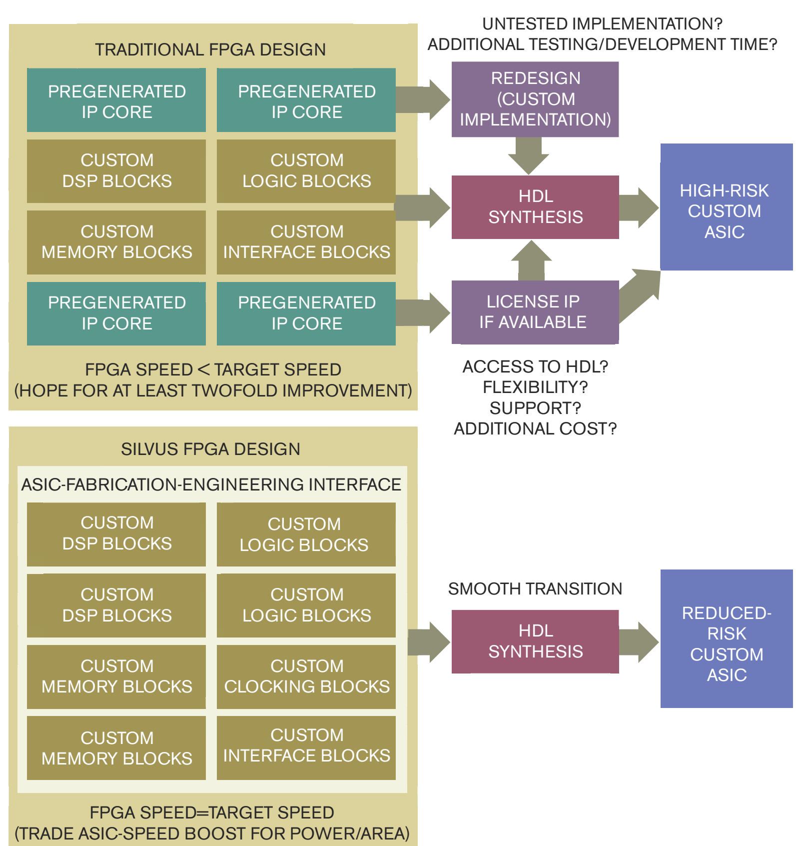

Figure 1 Companies such as Silvus Technologies have established a set of "siliconization"-design and HDL-coding guidelines to ensure the swift and seamless porting of an FPGA design to an ASIC.

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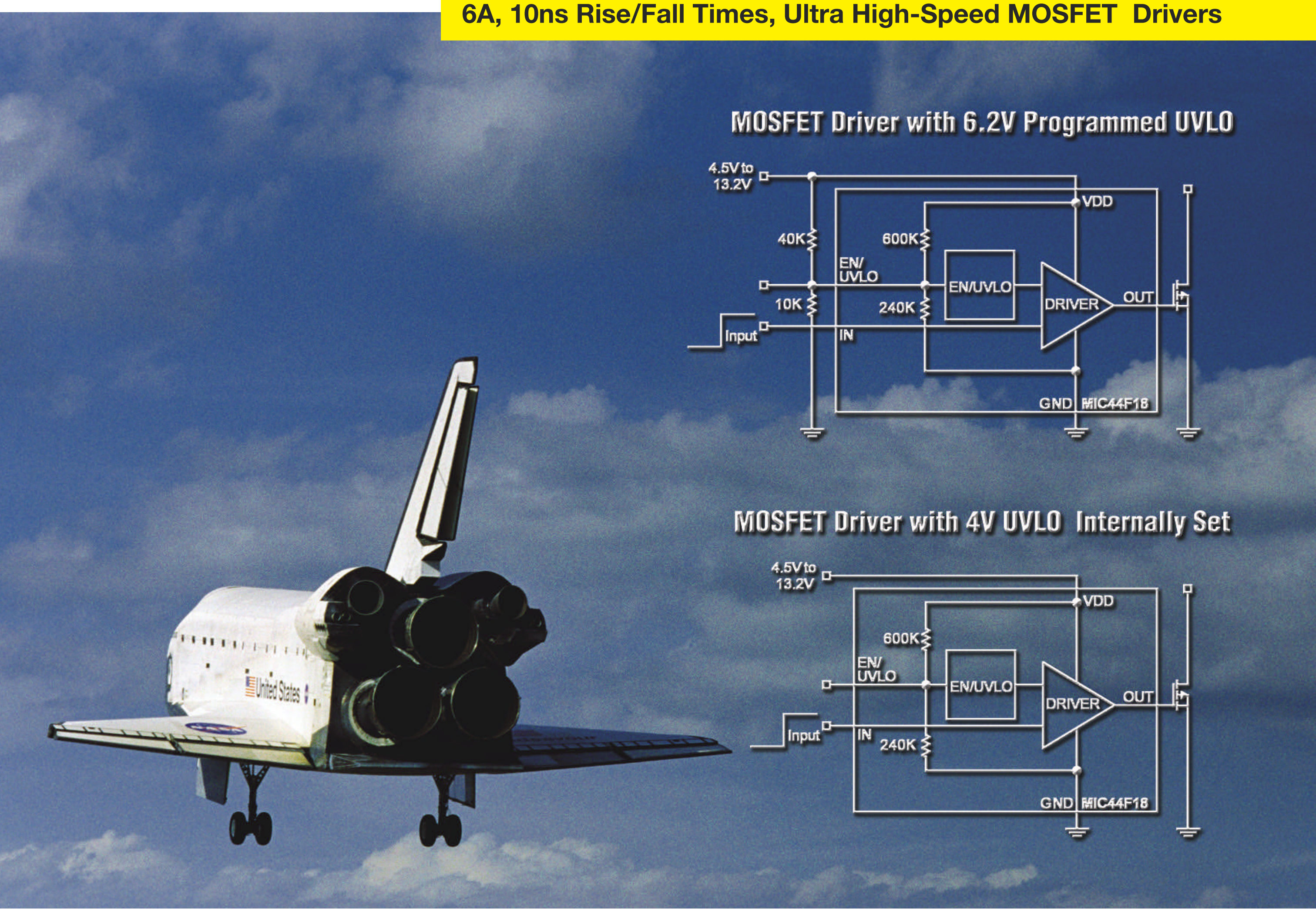

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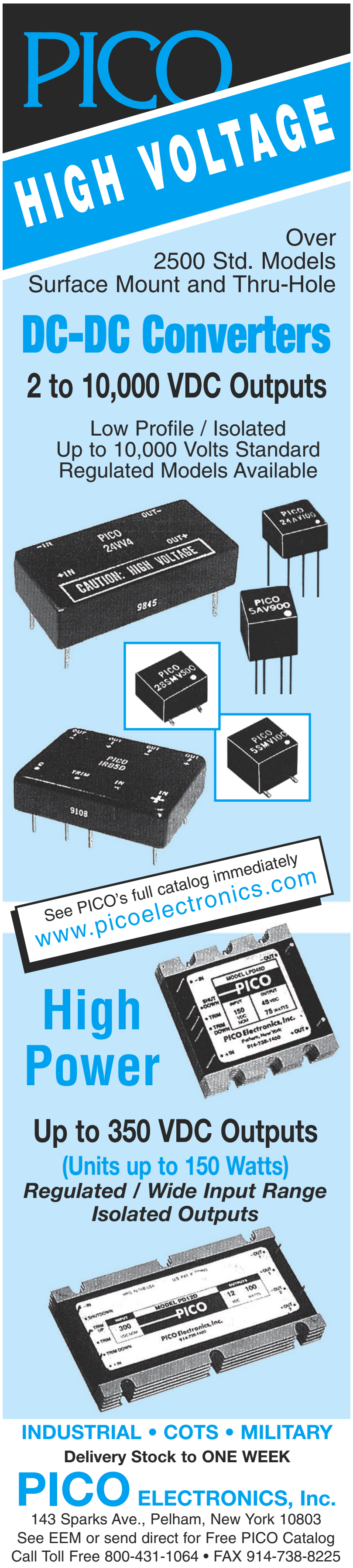

addition to reducing tapeout risk, potentially saving approximately $1 million to $3 million in total design cost per iteration.

Perhaps an even more important consequence of an FPGA design that runs at the speed of its target application is that any performance increase in the design due to migration from an FPGA to an ASIC directly increases the design-speed margin. Instead of using ASIC technology to "catch up" to the target speed, a chip designer looking to integrate the MAC and PHY blocks into a larger system now possesses a generous performance margin to play with to maximize power efficiency, which is crucial to the viability of a wireless system. The unrelenting scale-down of modern semiconductor-fabrication technology deep into the submicron world has turned circuit-leakage power into a major design consideration. Transistor-leakage currents in the form of subthreshold conduction between source and drain and both gate-oxide and junction tunneling have become major contributors to overall system-power dissipation: approximately 10% for 0.13-micron technology and rapidly increasing with each generation (**Reference 2**).

To combat this now-infamous implementation challenge, ASIC designers have turned to multiple-supply and multiple-threshold design techniques. In their advanced technology families, the leading foundries have allowed the designer access to double- and even triple-gate-oxide technologies. This access enables a mixed-threshold design, inside which the designer may choose from multiple types of transistors to minimize leakage. Designers may use thin-gate-oxide devices with higher speeds and lower switching thresholds to significantly improve the critical-path performance of the system. Although these devices generate more static-power dissipation in the form of leakage currents, they usually make up a small percentage of the overall design. The designer then places thick-gate-oxide devices with lower speeds and higher switching thresholds everywhere else in the design to maximize power savings—a step that can translate into tremendous energy savings. Unfortunately, such a mixed-threshold design requires careful analysis because modifications to the current critical path can lead to the emergence of new ones. An FPGA design that requires no speed increase to function at maximum performance can hand its generous speed margin as an ASIC implementation to the SOC-integration engineer, who may simply be able to synthesize it with all thick-oxide devices and realize the maximum energy savings with minimum additional optimization effort.

DISCIPLINED HDL CODING

To ensure the swift and seamless porting of an FPGA design to an ASIC, designers must adopt a disciplined HDL-coding methodology. Some vendors have established a set of "siliconization"-design and HDL-coding guidelines. Strict adherence to these guidelines has yielded a unified design that can target an FPGA just as easily as it can an ASIC.

The initial rule involves the use of IP in the FPGA. The FPGA designer may wish to save initial development time by using pregenerated IP cores or HDL constructs, often from the FPGA vendor, which are not synthesizable with an ASIC-vendor library. These practices can indeed save time—on the FPGA—but the designer should strictly avoid them; they will quickly lead to FPGA designs that require significant redesign and patchwork after FPGA validation but before the design becomes acceptable for an ASIC implementation (**Figure 1**).

Designers should be sure to instantiate any vendor- or customer-specific components, such as memory modules or I/O buffers, in the highest top-level design entity. For example, use a pad-ring wrapper to interface all I/Os with the desired package contacts. This wrapper can include all tristate I/O buffers and associated registers with all input, output, and tristate-enabled lines tunneling up from the rest of the design. With all these FPGA-specific components at the top level, you can use global or generic constructs to select among components for an FPGA implementation or vendor-specific components for an ASIC target. You can use a similar strategy with memory modules. In addition to providing for easy vendor customization, this strategy gives the ASIC engineer the freedom to designate, for example, a FIFO-depth threshold above which synthesis selects an SRAM- instead of a register-based implementation. These types of

design methodologies may initially complicate a modular design, though, because design often requires the components of interest at the lowest level of the hierarchy. However, the benefit is worth the hassle because it allows the vendor to easily configure, drop in, and wire these components—which you should not synthesize from behavioral code—without error-prone modification of individual lower-level submodules.

CLOCKS, FLIP-FLOPS, AND RESETS

Playing around with multiple clock domains and clock gating yields additional power savings, but designers must again be careful of how the HDL is written. The dynamic-power dissipation of a block is roughly proportional to the frequency of its input clock, so one simple power-saving approach is to use slower clocks in blocks that do not require processing to occur as quickly. Such a scheme necessitates the use of a clock generator/manager circuit that, again, you should pull to the top level so it is visible to the vendor. Use clock gating to kill dynamic-power consumption of temporarily unneeded blocks, such as those in the transmitting chain when in receiving mode and vice versa, as well as local clock-tree buffers. Use clock multiplexers to accomplish this task—also instantiated on the top level. This methodology for the use of clock managers and multiplexers resonates with the theme of top-level visibility—for designer flexibility, vendor-specific components, and, in this case, clock-tree analysis.

As with any other good ASIC design, all flip-flops should trigger on the rising edge and use a global asynchronous reset. This approach will enable ASIC-scan-chain testing without logic changes. Avoid locally generated asynchronous resets, but when they are absolutely necessary, multiplex them with a scan-enable signal—which will select the global reset during a scan test—so that the flip-flops in question won't be untestable. Carefully monitor synthesis reports for inferred latches; they are unreliable and untestable via scan chains. Pull the global asynchronous reset, as well as any local resets and scan-chain-enable logic, to the top level so it is visible to the vendor for reset-tree analysis (**references 3** and **4**).

ELIMINATE SURPRISES

ASIC development is a tricky business. Poor design-for-ASIC practices and convoluted development flow only add to the risk of potential setbacks and additional cost. The key to success is to take nothing for granted. A design that works at the target application speed on an FPGA frees the ASIC engineer to work his magic with power and area savings. When it comes to complex systems involving multiple types of functional blocks, proper design and HDL-coding doctrine and the discipline to follow them can significantly reduce the risk at tapeout. You invariably lower the number of refab and test iterations and ultimately reduce development cost and time to market. An SOC designer looking to quickly drop a wireless system into his chip inevitably has to turn to an outside IP provider who has had the time and resources necessary to develop such a complex system. When it comes down to a choice between an IP option that a designer has thrown together on an FPGA without proper regard for the ASIC transition and a design that he has meticulously prepared, streamlined, and built for a single-step transition to ASIC, the choice is clear. **EDN**

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AUTHOR'S BIOGRAPHY

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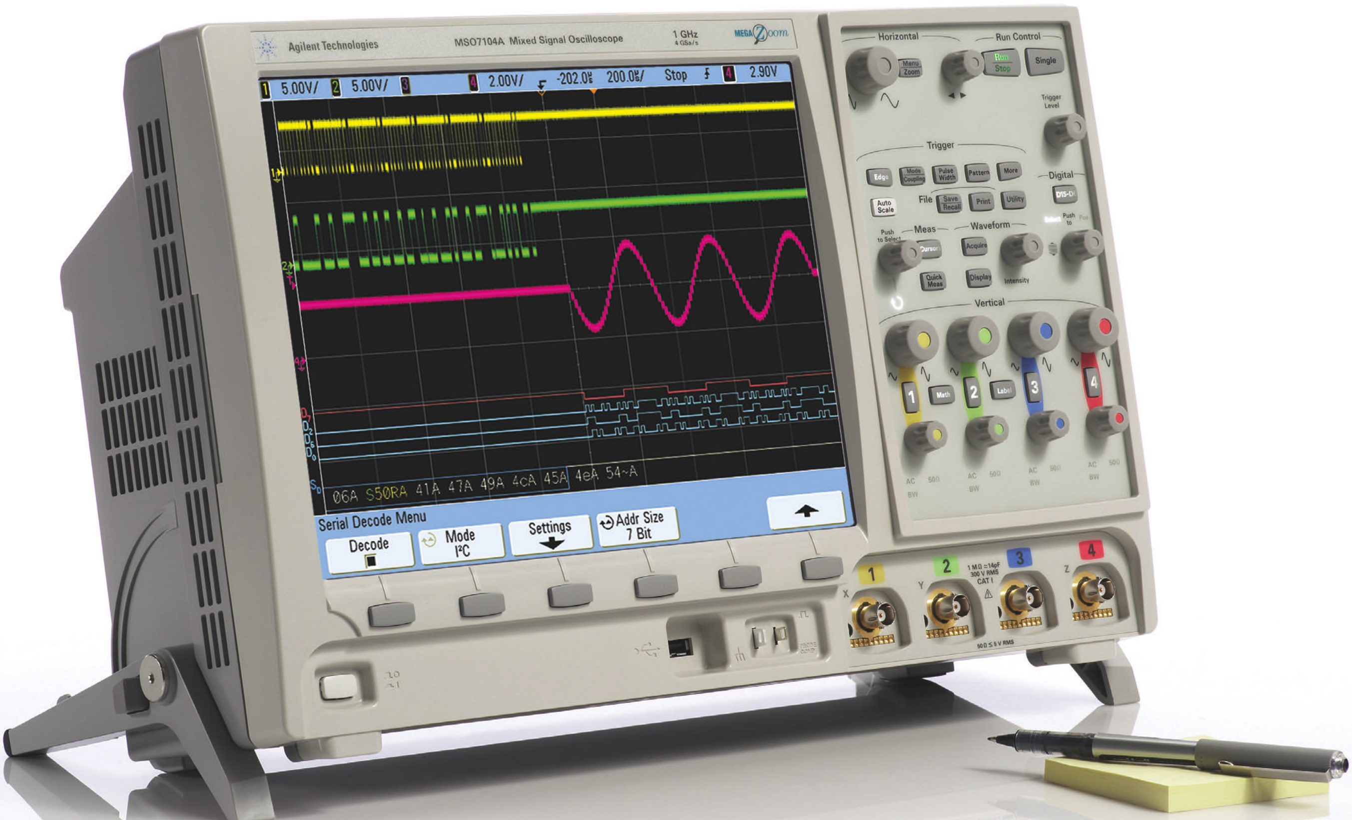

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BY PAUL RAKO • TECHNICAL EDITOR

In one of the earliest magnetic measurements, primitive mariners used lodestones—magnetized pieces of magnetite—to determine the earth's magnetic field. Today, thousands of applications require the measurement of magnetic fields. Instruments measure the B field, which engineers call magnetic-flux density, whereas physicists call the B field the magnetic field. According to US physicist and Nobel Prize winner Melvin Schwartz, "It is customary to call B the magnetic induction and H the magnetic field strength. We reject this custom inasmuch as B is the truly fundamental field and H is a subsidiary artifact" (**Reference 1**).

"A magnetometer cannot separate out this artificial distinction between the magnetic field, which is just what's produced by a coil, and total magnetic-flux density, which is produced by the coil plus by any internal current circulation inside, say, a piece of steel in the coil," says Bill Lee, PhD, owner of AlphaLab Electromagnetic Instruments, a supplier of diagnostic and laboratory products. "The rotating electrons in the steel produce magnetism there. All any magnetometer can read is the total flux density; it can't distinguish between the amount due to the coil and the amount due to magnetism of the core." Other fundamental issues with magnetic measurements are whether the field you are measuring is a dc or an ac field and whether you are measuring in just one axis or in multiple axes at once.

FROM MEDICAL TO MILITARY

Magnetic measurements find use in a variety of applications. For example, sensors in automobiles use the earth's field to help with navigation, and roadway sensors examine the magnetic signature of vehicles going by, determining the type of vehicle and its direction (**Reference 2** and **Figure 1**). In another application, geologists and earth-science researchers can detect iron-ore and other mineral anomalies by precisely mapping magnetic fields. By examining the latent magnetic field in rocks that have solidified over the ages, geologists can trace the changing location or frequent reversals of the earth's magnetic field (**Reference 3** and **Figure 2**). Some geological surveys use a fluxmeter, a simple coil pickup that connects to an integrator. When researchers pass magnetic materials through the fluxmeter and past a coil, an integrator inside the instrument calculates the dc field.

One of the primary military applications for magnetic-field measurement is detecting submarines. For example, the submarine-hunting Orion P3C military aircraft has a long tail boom to house the magnetometer far away from the engines and other sources of interference. Other military uses for magnetic measurements include instrumentation of small-caliber shells in the development of ranging fuses (**Reference 4**). The instruments inside the shell count the rotations of the shell as it spins through the earth's magnetic field. Because the magnetometer knows the turns ratio of the barrel rifling, a fuse circuit can calculate the distance the shell has traveled, so it can then burst over a target. Methods such as a time delay after firing are less accurate because the bullet speed varies with powder charge and gun condition.

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Countless other applications exist in the industrial, scientific, and medical fields. Industrial customers may simply need to verify the north and south poles on magnets used in motors. Paul Elliot, owner of magnetic-field-sensor-vendor Magnetic Sciences, reports that oil-pipeline installers need to measure the pipes to ensure that no latent magnetism resides in the steel. Many industrial users must measure the field of a magnet to ensure that it has not lost its strength. Another industrial use is to verify whether shipping containers are emitting a magnetic field that is greater than the legal limit.

Scientific uses of magnetic measurements include disk-drive-read-head research. The behavior of material in intense magnetic fields is an area of active study, and it is often necessary to measure the intense field that resistive, room-temperature, and superconducting magnets produce during research.

One of the most common medical uses of magnetic measurement is to verify the field uniformity in MRI (magnetic-resonance-imaging) machines. The field in the tunnel of an MRI machine must be uniform to parts per million. Sensitive instruments can measure the field at a point, but a sensor array that distributes

TOOLS ATTRACT ATTENTION

AT A GLANCE

- All magnetometers measure the B field, rather than the H field.
- Different sensors measure ac and dc fields.
- Some instruments measure in only one axis.
- Hall-effect sensors are versatile and have good resolution, but they drift over time and temperature.
- Instruments can cost pennies to hundreds of thousands of dollars.

24 to 32 sensors on an arc is more useful. Technicians rotate this sensor inside the tunnel of an MRI machine so that sensors sweep out in a sphere. If the magnetic field is uniform at the periphery of a sphere, the uniformity can only improve anywhere inside that sphere. In addition, magnetic sensors around an MRI machine block out the effects of passing cars or elevators. The sensor feeds back the signal to a 3-D Helmholtz coil, a device for producing a region of nearly uniform magnetic field. This coil ensures that outside influences do not affect the field inside the MRI tunnel.

Another area of medical research involves the susceptibility of humans to the magnetic fields that surround us. This area of study is more controversial because power lines and electric cars emit approximately 1-mG (milligauss) fields, whereas the earth's magnetic field is 500 mG. Still, MRI machines can be of concern to health-care workers who operate them. The ICNIRP (International Commission on Nonionizing Radiation Protection) guidelines for occupational static-magnetic fields are 200 mT (millitesla) for continuous exposure; 2000 mT for short-term, whole-body exposure; and 5000 mT for exposure to arms and legs, according to Ian J Walker, vice president of sales for sensor-distributor and -integrator GMW Associates. "These field levels are high and indicate the lack of evidence for biological effects from dc fields," he says (**Reference 5**).

The use of gaussmeters to measure magnetic fields in homes has uncovered another valuable application. Homes with 60-Hz fields often have wiring errors such that the neutral leg of the dc wiring returns through the ground wire or plumbing. The current conductors are far apart and form a loop, so they generate larger magnetic fields than those in properly operating wiring. Whether the fields themselves could cause injury is debatable, but it is always more desirable to have wall power in the wires and not the pipes of your home.

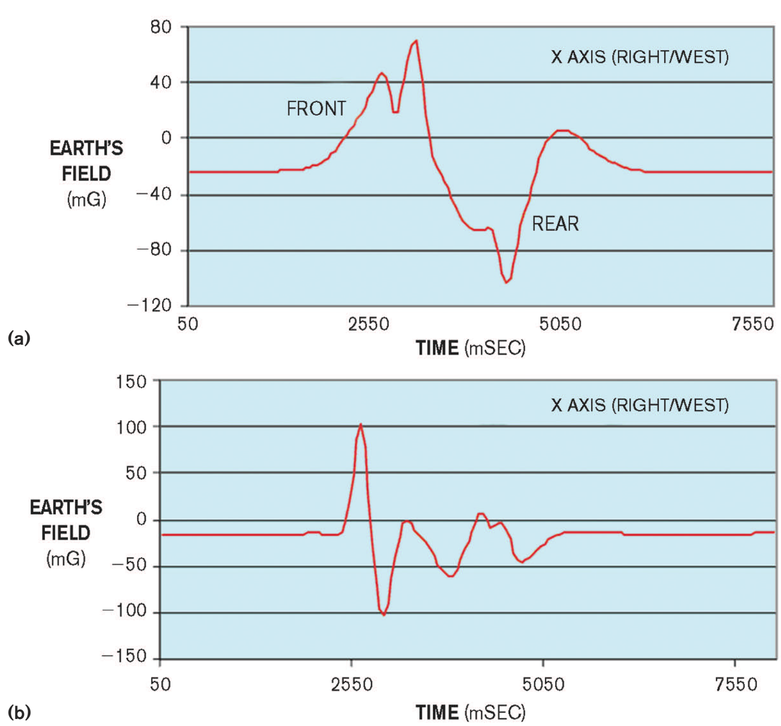

Figure 1 A magnetic sensor in the road can determine vehicle direction and type from a Silhouette van (a) and a Saturn sedan (b) (courtesy Honeywell).

SENSE AND "SENSORABILITY"

The availability of such a diverse array of magnetic measurements requires a wide selection of sensors to properly characterize the magnetic field (**Reference 6** and **Figure 3**). One of the most basic is a simple inductive sensor comprising a coil with a magnetic core. It can measure ac fields and may also pick up electric fields. The response of the core material also limits the upper frequency that the sensor can detect. These types of sensors find use in inexpensive gaussmeters, often targeting the health-care market.

The largest drawback of inductive sensors is their inability to measure dc fields. Hall-effect sensors overcome this problem. A Hall-effect sensor yields an output voltage proportional to the magnetic-field strength. Hall-effect sensors work in only one axis, but vendors can mount three devices together for three-axis measurement that provides enough information to detect the earth's magnetic field or, just as useful, to subtract it from the real dc field of interest. The downside of these sensors is that they drift over time and temperature, making accurate measurements difficult.

Flux-gate sensors, which indicate the direction of the earth's magnetic field, can also measure dc fields and can be more sensitive than Hall-effect devices. A flux-gate sensor works by using an ac electric current to sweep a permeable core through its magnetic-saturation curve. The property of the core determines how many ampere-turns—the magnetomotive force developed by a coil through which a current flows—are necessary to achieve saturation. The presence of a dc field in the core reduces the amount of current necessary to achieve saturation in one magnetic direction and increases the current necessary when you try to drive the core in the opposite magnetic direction. It is easy to measure small currents, and, as such, it is possible to measure small fields (**Reference 7**). If you excite the flux gate fast enough, it can easily meas-

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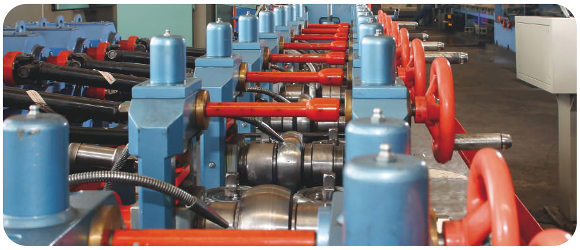

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Figure 2 This field researcher is using a Grad601 flux-gate gradiometer at an archeological-dig site (courtesy Bartington).

ure 60-Hz fields and other ac fields into the audio range.

Texas Instruments' Burr-Brown division offers the DRV401 chip, which both excites and measures the response of the core in a magnetoinductive magnetometer, similar to a flux gate. By driving the core to a certain current and then reversing, the part establishes a natural oscillation. With no applied magnetic field, the duty cycle of the oscillations is precisely 50%. With an applied external field, the duty cycle changes, showing both the magnitude and the direction of the applied magnetic field. The frequency range of this technique extends to 100 kHz. This chip provides the magnetic sensing in current sensors for magnetic-product manufacturer Vacuumschmelze.

A broad range of magnetic sensors uses the principle of magnetoresistance. A magnetoresistive material changes its resistance in the presence of a magnetic field. Irish physicist and engineer William Thomson, more commonly known as Lord Kelvin, in 1856 discovered the theoretical basis for the phenomenon, and later development of technologies allowing the deposition of thin metallic films popularized these sensors. Because the field directly changes the resistance, this class of sensor can measure both dc and ac fields, and, because the sensors are resistive, you can use them at high frequencies, which accounts for their use in disk drives. These sensors can employ AMR (anisotropic-magnetoresistance), GMR (giant-magnetoresistance), or TMR (tunneling-magnetoresistance) techniques. Japanese physicist Terunobu Miyazaki discovered in 1995 that you can use the TMR technique at room temperature. Since the emergence of that breakthrough, manufacturers of disk-drive-read heads have adopted TMR sensors to reach the fast response and high bit rates that modern drives require. AMR sensors, available from Honeywell and

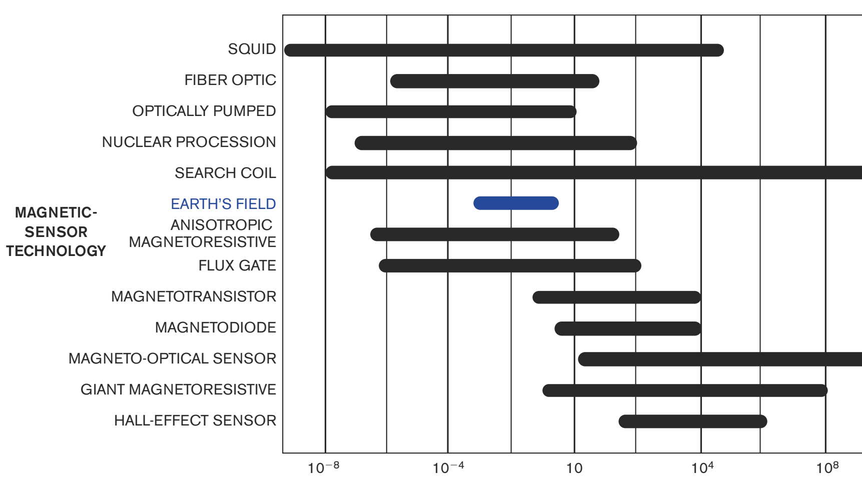

Figure 3 The sensitivity ranges of various magnetic sensors span many orders of magnitude (courtesy Honeywell).

Figure 4 Inductive-sensor instruments can measure only ac fields (courtesy AlphaLab).

Figure 5 The FW Bell model 6010 single-axis dc gaussmeter achieves ±0.25% dc accuracy (courtesy Sypris).

others, find use in anything from compasses to gear-tooth detection.

For example, Maxim offers the 16-bit, RISC-microcontroller-based MAXQ-7665 smart data-acquisition system that interfaces to magnetoresistive sensors; it also integrates an analog front end, a programmable-gain amplifier, and bridge excitation. The device measures the steering angle for yaw and traction control in automotive applications. The microprocessor core has a multiply/accumulate instruction, allowing the device to perform calculations and DSP-type filtering, according to Mike Mellor, staff engineer at Maxim. The device also integrates a CAN (controller-area-network) bus and UART.

Sensors employing NMR (nuclear-magnetic-resonance) technology base their measurement on atomic properties, so they are highly accurate, and you can use them as primary standards. Their resolution approaches one part per billion, and their resonance is based on the spin states of a proton in a hydrogen nucleus. The proton-procession magnetometer subjects water or other hydrogen-rich samples to an intense magnetic field and then allows the field to collapse; a second inductor then measures the weak resonance of the protons. The magnetic field of the earth would result in a resonant frequency of 1.5 kHz. The Overhauser type of NMR sensor excites the hydrogen atoms in water with RF energy of nearly 45 MHz; the sensor absorbs energy at resonance, and this frequency is proportional to the magnetic field. The measurement is precise, has no drift, and measures the three-axis field because the effect is nondirectional. These sensors are more expensive than the other types, however, and have a unique drawback: The water inside freezes in cold climates and ruins the internal vessel, according to Brian Richter, president of GMW Associates. This scenario could happen, for example, if a user leaves the sensor on an airport runway in a frozen climate. NMR sensors also need a uniform field across the measuring vessel, and they work only on dc and slow-ac fields.

The most sensitive magnetometers are SQUIDs (superconducting-quantum-interference devices). "They can easily detect the magnetic field from the nerve impulses in your brain or your heart," says AlphaLab's Lee. "You have to shield them very well since a truck driving by a half-mile away can add more magnetic fields."

WEIGHING YOUR OPTIONS

Selling for less than \$300, inductive-measurement devices are the most economical (**Figure 4**). You use them to measure the magnetic fields from ac sources, such as power lines and motors. These instruments can also help find wiring breaks because the magnetic field collapses when it encounters the broken wire. Inductive sensors come in both single-axis and triaxis versions. For example, the FW Bell division of Sypris Test and Measurement offers the series 4100 meters, which can measure ac fields at frequencies higher than 25 Hz in three axes. One unit in the series, the Bell-4180, sells for \$324.

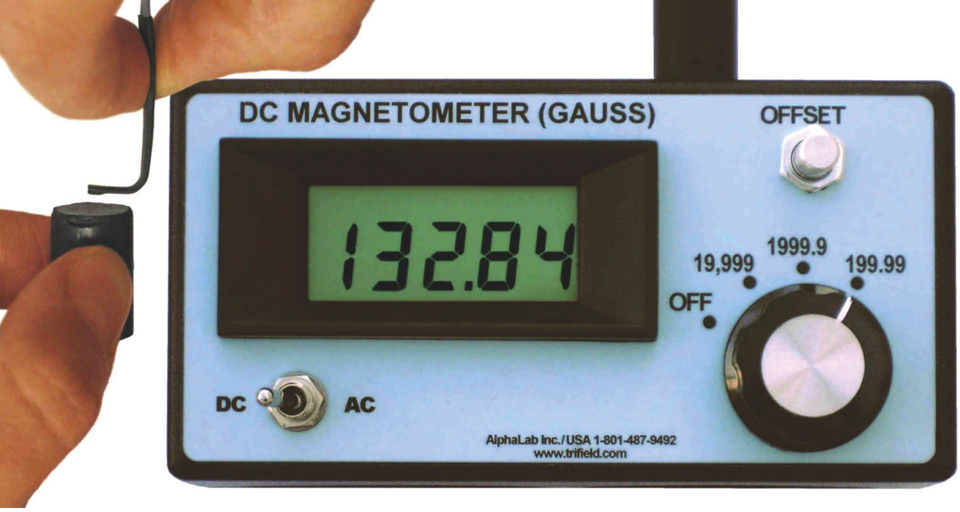

Figure 6 You can bend the sensor for this magnetometer into an L shape or keep it straight. It will withstand 1000 flexures (courtesy AlphaLab).

If high sensitivity is a necessity for your application, you may want to consider a flux-gate sensor. For example, the Mag-03MC flux-gate-magnetometer probe from Bartington Instruments has 70- to 1000-μT sensitivity; this three-axis, dc to 3-kHz instrument has ±0.5% accuracy. The probe, available from GMW Associates, costs $3190 and interfaces with the Mag-03DAM digitizer, which sells for $5750. GMW Associates provides National Instruments LabView drivers for this device and other magnetometers.

Hall-effect sensors are more versatile and their prices—$500 to $800 for a single-axis device and more than $1000 for a three-axis unit—reflect this feature. The FW Bell 5100 series Hall-effect sensor measures dc fields, has 2% accuracy, and can measure frequencies as high as 20 kHz at 1G to 20 kG. The model 5180 has 1.1% accuracy, measures frequencies as high as 30 kHz, and ranges to 30 kG. It also has peak hold, relative mode, and analog and USB outputs. The 5180 costs $1325, and another unit in the series, the 5170, sells for $985. FW Bell also makes two benchtop instruments. The model 6010 Hall-effect gaussmeter sells for $2492, and the 7010 single-channel gaussmeter/teslameter costs $4365 (**Figure 5**). The 7010, with an accuracy of ±0.5% dc ±2%, can simultaneously measure and display flux-density, frequency, temperature, minimum, maximum, peak, and valley parameters. The three-channel model 7030 gaussmeter/teslameter sells for $6864.

You can use AlphaLab's $380, 10,000G DC magnetometer, with overall accuracy of ±2% at 30 to 110°F, for both dc and ac measurements (**Figure 6**). The unit has a pseudo-root-mean-square response, and it operates at 45 to 2000 Hz. A high-stability version is also available. The meter comes with a NIST (National Institute of Standards and Technology)-traceable-calibration certificate. Another line of meters, Hirst Magnetic Instruments' gaussmeters, includes the Hall-effect VGM01, which connects to your PC through an RS-232 interface. Metrolab's $3980 THM1176 sensor integrates three orthogonal Hall-effect elements onto one IC (**Figure 7**). The USB instrument provides a 0 to 20T field range, a dc to 1-kHz passband, a three-axis Hall-effect sensor in a 193.54-mm^3 footprint, and a USB interface that can also interface to an optional $1730 PDA (personal digital assistant). Both the sensor and the PDA include software and are available from GMW Associates.

The Chen Yang Technologies CYHT-201 measures dc or ac magnetic fields. The instrument has ±2% dc accuracy and ±5% ac accuracy, measures dc to 200-kHz fields, and has a 4½-digit LCD. The company also offers the $350 CYHT-T08A gaussmeter with a Hall-effect probe. Yet another handheld teslameter comes from Tel-Atomic. The TeslaMeter 2000 costs $719 and comes with a transverse probe. The Hall-effect device measures sensitivity to 2T. Accuracy is ±0.5% for dc measurements and ±2% for ac measurements. The company also offers a $150 axial probe and is developing a triaxial probe. Lake Shore Cryotronics offers the $590 Model 410 handheld gaussmeter for field measurements of 0.1G to 20 kG (0.01 mT to 2T). The device displays measurements in gauss or tesla and ac- or dc-magnetic-field values with resolution to 100 mG. Operating functions include maximum hold, filter, relative reading, zero probe, and an audible alarm. Accuracy is ±0.1% full-scale dc and 5% ac, and the frequency response extends to 10 kHz. For users needing a small, inex-

Figure 7 This three-axis Metrolab probe has USB output and comes with an optional PDA (courtesy GMW Associates).

pensive dc gaussmeter, Carlsen Melton offers the $329 GM-200A, which measures to 10,000G with 2% accuracy and resolution of less than 1G. A calibration certificate costs $50.

At the other end of the pricing scale for Hall-effect meters, Group3 Technology's $4390 DTM-151 teslameter has 20-bit resolution and ±0.01% accuracy of full-scale for dc or slow-dc fields. For less demanding applications, the $2380 DTM-133 with digital-linearity correction has 0.03% accuracy, resolution to 10 ppm, and a temperature stability of 100 ppm/°C. Both devices are available from GMW Associates. Because these Hall-effect devices drift more than an NMR unit does, customers sometimes buy one NMR instrument to verify the calibration and drift of several of these less expensive Hall-effect meters.

Micro Magnetics' TMR sensors can investigate extremely small areas. The die measures 1.9×1.9 mm, but the actual area that senses the magnetic field measures only a few microns across, according to Ben Schrag, project manager of metrology at the company. He also notes that you can make an array of sensors on one die and average the result to get better sensitivity. The $325, bipolar, linear-output STJ-020 magnetic microsensor has a field sensitivity of 5 nT. Because the circuit comprises only resistors, the sensor has a frequency response as high as 5 MHz. Sensors with lower resistance have frequency response exceeding 100 MHz.

Metrolab's NMR-type PT 2025 sensor finds extensive use in medical-MRI applications (**Figure 8**). The teslameter achieves 5-ppm absolute accuracy and 0.1-μT (1-mG) resolution for measuring or mapping uniform magnetic fields of 0.043 to 13.7T (430G to 137 kG). Optional probe multiplexers enable readout of as many as 64 probes. The instrument operates in MRI- and spectrometer-magnet mapping, precision field control, and magnetic-sensor calibration. The PT 2025 instrument, for dc or slow, low frequencies, costs $20,650 and is available from GMW Associates. The $31,580 MFC 3045D-32 NMR-probe array, also available from GMW Associates, sweeps a sphere and characterizes the field-strength uniformity for MRI markets.

Magnetoresistive sensors measure weak-dc fields in AlphaLab's dc milligauss magnetometer. The instrument has a resolution of 0.01 mG (1 nT) and a range of ±2000 mG (200 mT). At fixed temperature, reproducibility is ±0.01 mG (1 nT), and the temperature coefficients of the offset and of the gain are less than 0.01 mG/°C and less than 0.0015%/°C, respectively. The $490 device has a gain accuracy of ±0.5%, and the meter offset is ±0.5 mG. The $4.95 CY-MVF555 magnetic-field viewer from Chen Yang requires no electricity and allows you to directly view a magnetic field (**Figure 9**). This ability can expose multiple poles in a magnetic assembly or indicate the field uniformity or fringing around a magnet.

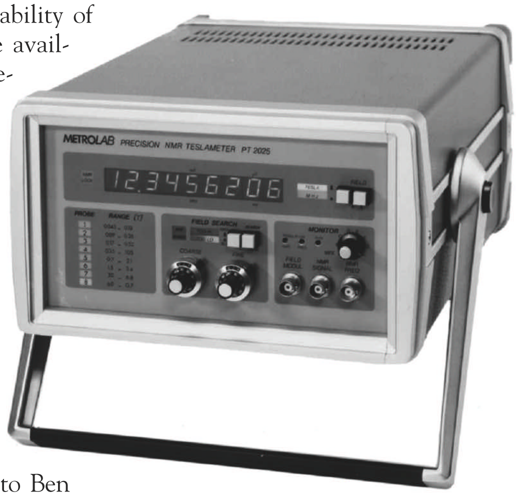

Figure 8 This NMR gaussmeter offers 5-ppm accuracy but can measure only dc or very-slow-ac fields (courtesy Metrolab) and comes with an optional PDA (courtesy GMW Associates).

Magnetic measurements are important if you are finding the North Pole or looking for submarines underwater. Instruments to measure magnetism can detect a dozen orders of magnitude of field strength. Understanding whether you need to measure ac or dc fields, along with the limitations of single- versus three-axis measurements, will help you do the job. If you realize the limitations of the various sensors and instrument types, you can ensure that you get an accurate measurement in the most cost-effective way.

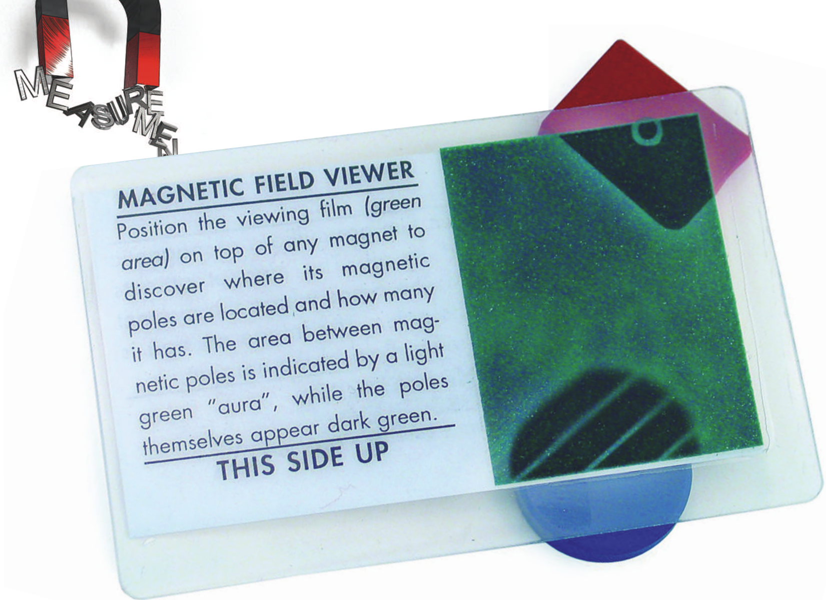

Figure 9 This viewer can directly display the presence of magnetic poles (courtesy Chen Yang).

No matter whether your instrument costs \$50 or \$50,000, it represents a beautiful collaboration of the regimes of physics, electronics, and even optics. EDN

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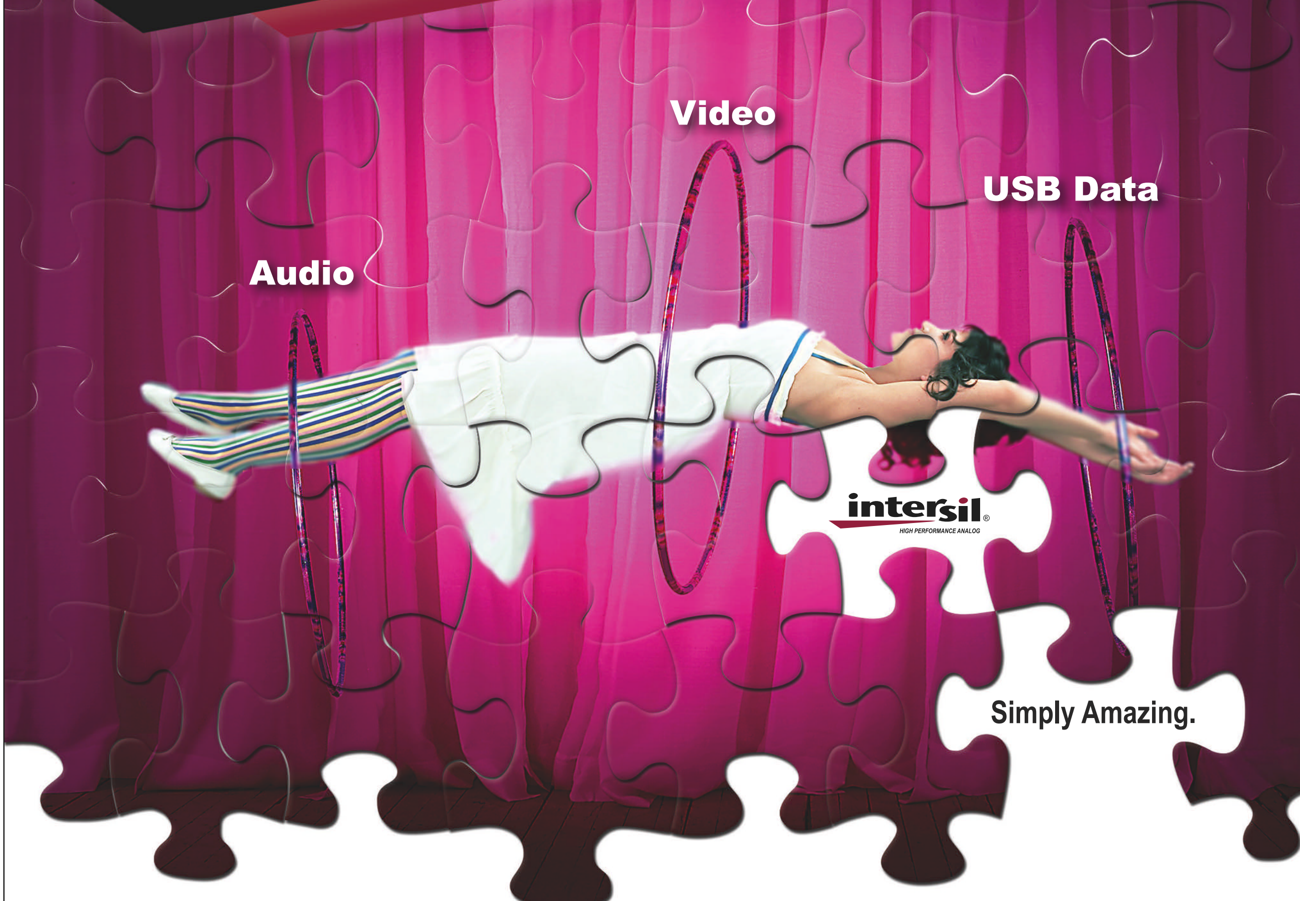

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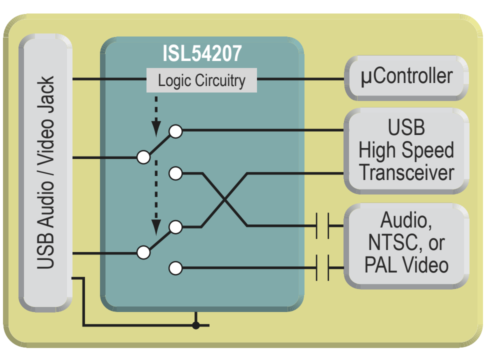
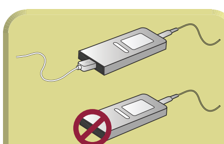
ISL54415	0.007	12	0.04 / 0.03
ISL54416	0.007	12	0.04 / 0.03
ISL54417	0.007	12	0.04 / 0.03





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Device	Audio THD 32Ω (%)	USB Speed
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ISL54206	0.06	480
ISL54400	0.007	12
ISL54401	0.007	12
ISL54402	0.007	12

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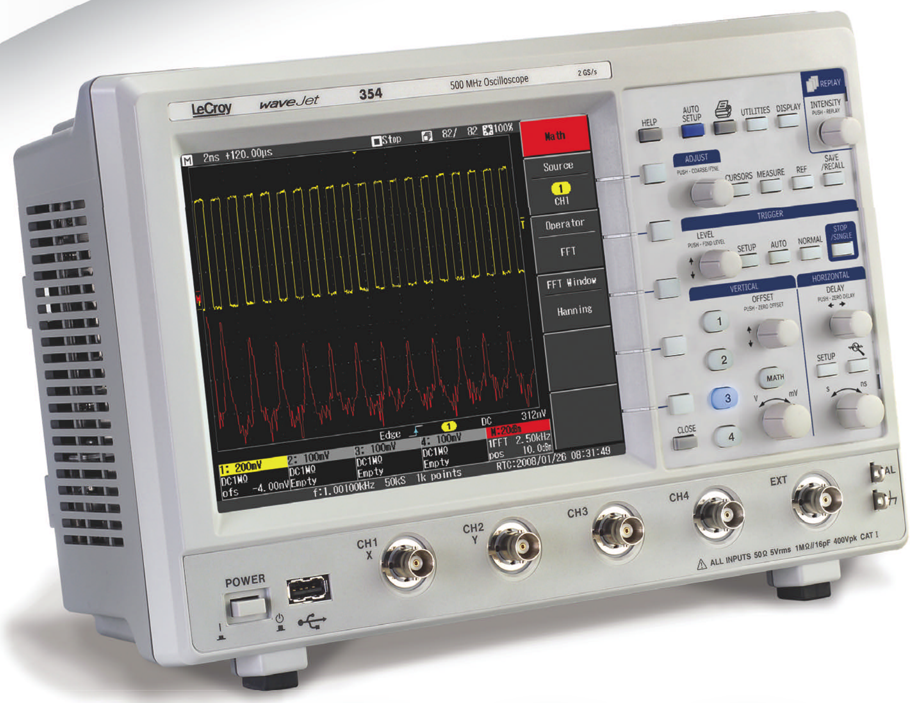

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Spread-spectrum-clock generators reduce EMI and signal-integrity problems

AS ELECTRONIC PRODUCTS BECOME FASTER AND MORE COMPLEX, RADIATED-EMI EMISSIONS INCREASE DRAMATICALLY. WITH THE RECENT PROLIFERATION OF PORTABLE AND WIRELESS PRODUCTS, THIS GROWTH HEIGHTENS THE PROBABILITY OF INTERFERENCE BETWEEN SYSTEMS AND MAKES EMI A MAJOR CONCERN.

It is well-known that, during system development, critical signal-integrity and EMI (electromagnetic-interference) simulations are difficult, time-consuming, and error-prone due to their reliance on hard-to-predict models and parameter extractions. This situation worsens with every new product generation due to steadily increasing clock speeds and decreasing supply voltages, resulting in reduced noise margins. These problems, coupled with the shorter product-development periods that shorter product-life cycles require, hinder the ability of designers to bring their products to market fast enough to meet market demand. The ever-increasing expectations of the end user or the consumer require approaches to such problems that interfere with a company's ability to expeditiously manufacture quality products at high volumes and to outpace dwindling product life spans in the market.

Although simulating electronics systems to predict EMI levels is a difficult and time-consuming task, understanding the fundamental causes of electromagnetic radiation is simple. Any charge moving in an electrical field or change in a field emits electromagnetic radiation. The strength of radiation is directly proportional to the rate of change. The sources of electromagnetic emissions can be intentional transmitters, such as cellular phones. But digital systems, such as PCs, PDAs (personal digital assistants), printers, and scanners, emit unintentional radiation. In digital systems, periodic clock signals are the major causes of EMI radiation. In addition, control and timing signals, address and data buses, interconnect cables, and connectors also contribute to EMI emissions.

The two main modes of electromagnetic radiation are the differential mode, the result of local current loops between PCB (printed-circuit-board)-interconnect traces and the ground planes, and the common mode, the result of the coupling of ground and power-plane noise into traces, I/O buses, and cable lines. Fundamental and odd multiples of fundamental sinusoidal frequencies, or harmonics, generate a square wave. EMI radiation increases with higher edge speeds (rise and fall times) and higher drive levels. Harmonic frequencies set the exact location of the radiation spectrum and the clock-signal

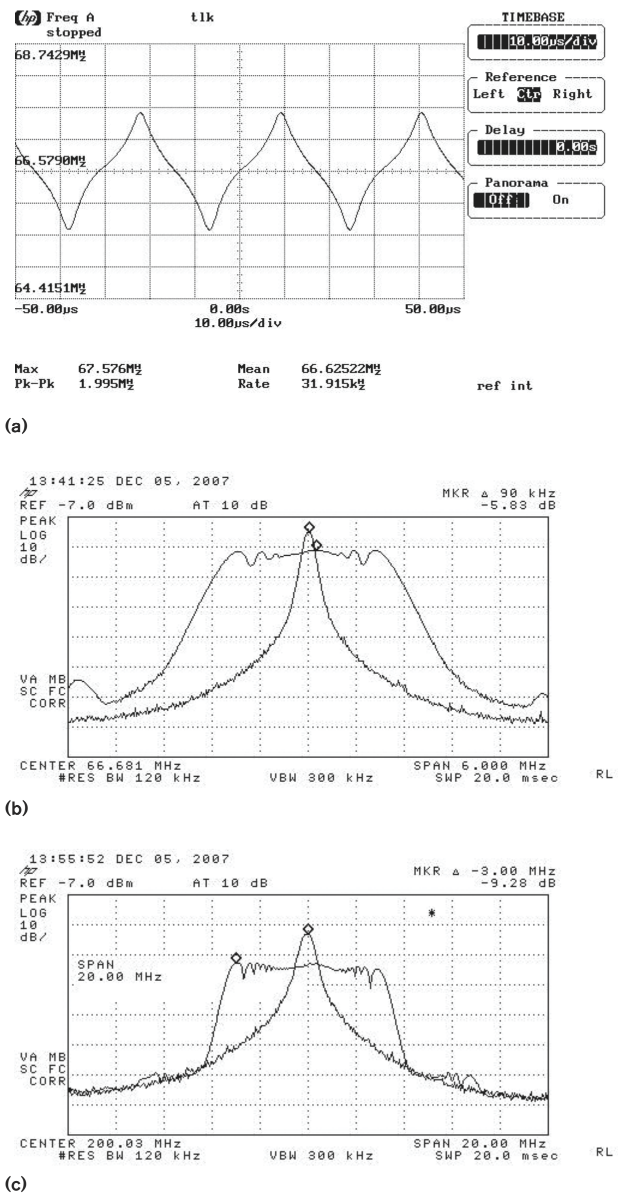

Figure 1 A Lexmark Profile of a modulated 66.666-MHz system clock (a) shows the relative EMI reduction for fundamental (b) and third-order harmonics (c).

edge speeds, and drive levels set the bandwidth, or radiation strength, of each harmonic.

Shielding is a relatively simple way to reduce EMI emissions by containing them within the system and fully or partially covering the emission locations with grounded conductive shields. Shielding could be an effective approach in systems with strong emissions in which space, weight, and cost are unimportant. In most systems, however, especially portable and handheld products, shielding becomes the least desirable method of EMI reduction. Shielding increases the size, weight, and cost—creating a substantial increase in labor costs, for example, because the shielding of these products is difficult to automate in manufacturing.

Designers widely employ lowpass filters to reduce EMI emissions that clock and timing signals generate. They reduce rise and fall times by filtering out higher-order harmonics. But this option might not be viable in high-speed systems because such filtering both reduces the critical setup-and-hold-time margins and increases signal overshoot, undershoot, and ringing. A major problem with filtering rests on the fact that this technique is not systemic, meaning that reducing EMI emission at any given node in the system does not reduce the emissions in the other nodes. Because designers start with little information, they must provide filter placement in many suspicious locations, wasting valuable time and PCB space.

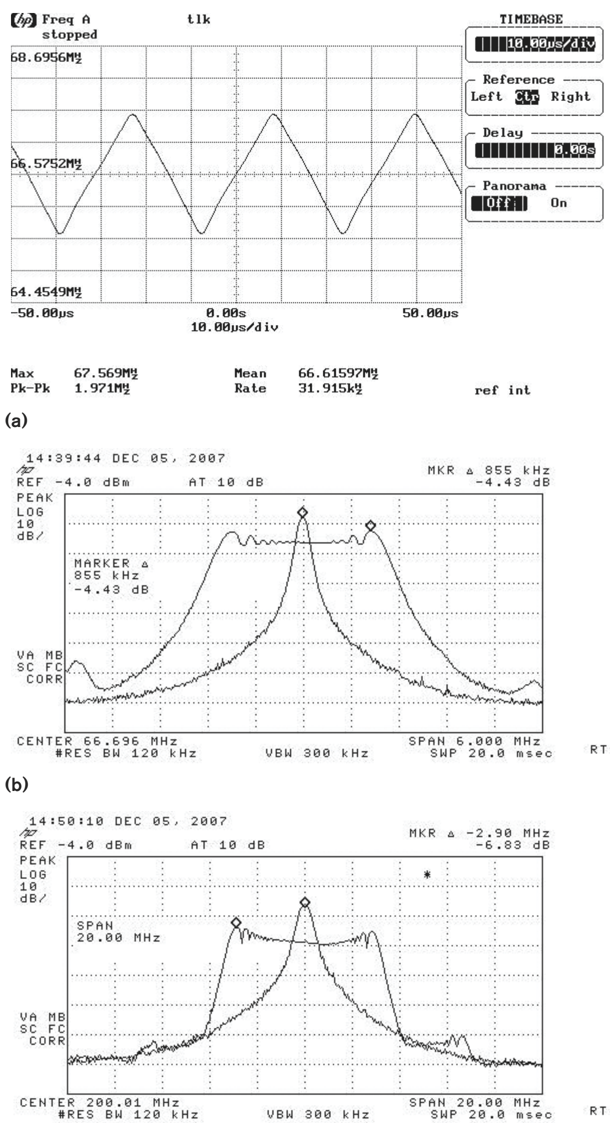

Figure 2 A triangular profile of a 66.666-MHz system clock (a) with a ±1.5% center spread shows similar relative-EMI reductions for fundamental (b) and third-order (c) harmonics.

SPREAD-SPECTRUM CLOCKS

A more effective and efficient approach is to use SSCG (spread-spectrum-clock generation) to control and reduce EMI emissions. Instead of maintaining a constant frequency, the SSCG technique modulates the system-clock frequency with a much smaller frequency—typically 30 to 90 kHz—to control and reduce EMI emissions at their source, the system clock. The systemic nature of SSCG has a major advantage over other EMI-reduction techniques because all clock and timing signals you derive from the spread-spectrum clock are also modulated at the same percentage, leading to a dramatic EMI reduction throughout the system.

SSCG can reduce the radiated emissions of the digital-clock and -timing signals. You achieve EMI reduction by frequency-modulating the system clock with a low-frequency signal. This approach creates a frequency spectrum with sideband harmonics. Intentionally broadbanding the narrowband repetitive system clock simultaneously reduces the peak spectral energy in both the fundamental and the harmonic frequencies. The MF (modulation frequency) is usually 30 kHz, large enough to stay above the audio band yet small enough to avoid timing and tracking problems in the system—typically at less than 90 kHz.

Figure 1a shows the Lexmark Profile, a typical nonlinear-frequency profile, which Lexmark International patented (**Reference 1**). In this example, a unique, 32-kHz, nonlinear-frequency profile modulates a 66.666-MHz system clock using ±1.5% frequency-modulation limits. Because the modulation centers on 66.666 MHz, this type of profile is known as center-spread-frequency modulation. **Figures 1b** and **1c** show the amount of relative EMI reduction on the same clock using ±1.5% center spread in reference to an unmodulated system clock for fundamental and third-order harmonics. **Figure 2** shows the

TABLE 1 PROGRAMMABLE PARAMETERS AND RANGES FOR THE SL15100

Programmable parameter	Range	Resolution
Output-to-output skew (psec)	−160 to +160	20
Output-drive strength (Ω)	20 to 100	20
Output-rise/fall times (15-pF clock)	0.3 to 4.2 psec	0.3 nsec
Duty cycle (%)	−3 to +3	1
Frequency	1 to 200 MHz	2 ppm
Spread-spectrum amplitude (%)	0 to 5	0.05
Spread-spectrum modulation (kHz)	16 to 128	1

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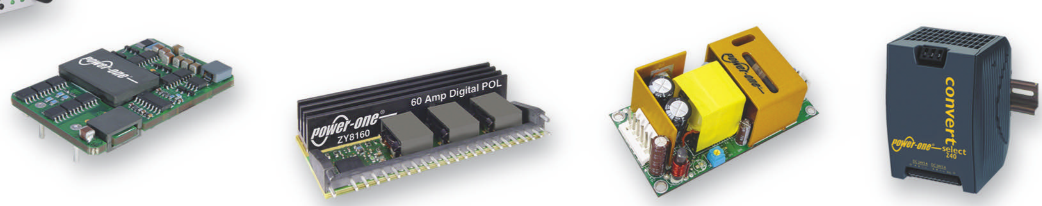

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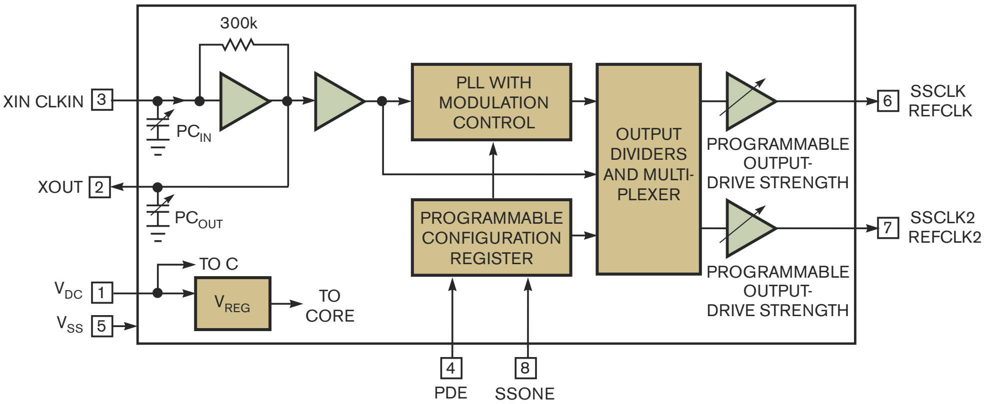

Figure 3 Users can dynamically update the SL15100 spread-spectrum-clock generator using the programmable configuration register.

same 66.666-MHz system clock with the same ±1.5% center spread and relative EMI reductions for the same harmonics using the triangular profile. The SSCG technique is analogous to the spread-spectrum technique in communications applications. However, it does not spread encoded information over a wide bandwidth, as CDMA (code-division multiple access) does, and the only benefit of using SSCG is to reduce undesired EMI emissions.

PROGRAMMABLE GENERATORS

The major advantage of using a programmable SSCG, such as the SpectraLinear (www.spectralinear.com) SL15100 (**Figure 3**), is that it improves and optimizes various timing specifications within the system-timing budget. One of the most critical considerations of clock-signal integrity is the matching of the impedance of the board trace and driven load to the clock driver. This matching ensures that the clock signal is free from overshooting or undershooting and ringing for each of the driven clock signals. Programmable clocks achieve this goal by providing adjustable impedance levels at each clock-output driver to ensure a good match to various load-impedance levels. Programmable-clock-drive-strength levels allow the user to match load-impedance levels at each output, to obtain matched impedance levels, and to optimize the signal integrity based on the actual levels the user measured during system evaluation. In addition, you can use the programmable-drive levels to control clock-signal rise and fall times within acceptable signal-integrity limits to slow the edges, which reduce high-frequency harmonic content and further reduce EMI. **Table 1** shows programmable parameters and ranges for the SL15100.

Frequency margining is the stepping up or down of output

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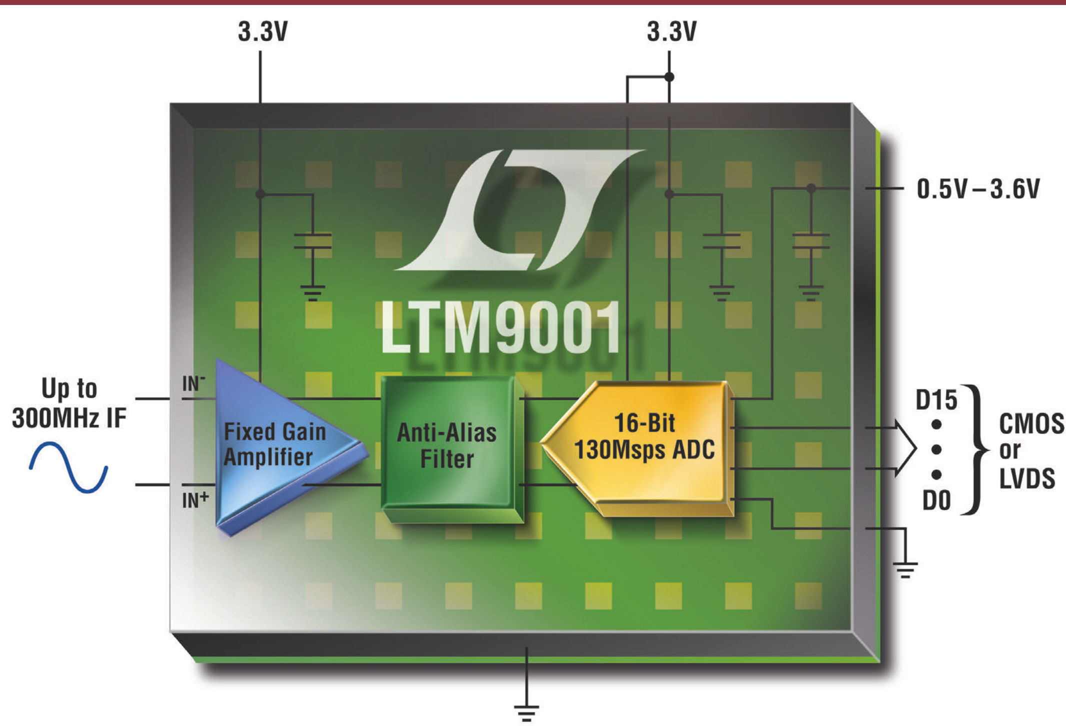

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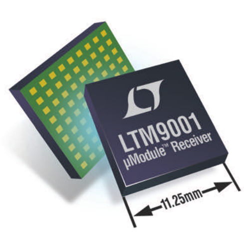
- 11.25mm x 11.25mm LGA Package

LTM9001: 16-Bit IF/Baseband Receiver Subsystem



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frequency through frequency-control pins or the I^2C (inter-integrated-circuit) interface. The technique is both useful and easy to implement under automated-testing systems to find potential system weaknesses and failures during the product-development and production phases. The fine, gradual increase or decrease of the system-clock frequency sweeps the range of the frequency to detect any irregularities or failures for a given frequency range, and you could easily implement it using programmable clocks by setting both center- and extreme-frequency limits for changing system requirements. In addition, you can test the margin of other critical timing parameters, such as clock skew, spread amplitude (percentage), or spread-modulation rates, to verify that the receiving PLL (phase-lock loop) in an ASIC or other system-component interface has sufficient built-in bandwidth and timing margins.

Programmable clocks are also beneficial during EMC (electromagnetic-compatibility) testing because you can easily set frequency modulation to any value from 0 to 5%. This programmable attribute of SSCG simplifies compatibility measurements during design and testing, eliminates product-introduction delays, and improves time to market. The second benefit of SSCG is reducing EMI without degrading the timing-signal quality. The system references setup-and-hold times to only the rising edge of the timing signal. Because the rise and fall time changes only by the amount of spread percentage when you use a spread-spectrum approach, the process maintains the critical setup-and-hold-timing margins.

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Another benefit of using SSCG is that you can integrate additional programmable EMI-reduction and -timing functions into the same product, further enhancing system performance and reducing costs. Multiple-PLL and multioutput-SSCG products with selective use of spread-spectrum-clock functions enable users to integrate many functions, such as buffers and level translators. Using multiple unique programmable-frequency outputs in the same product eliminates a large number of crystals and crystal oscillators by using a single-standard, first-order crystal, saving additional cost and PCB space.

Even in systems meeting EMC requirements, SSCG could further reduce the emission levels to reduce the total number of PCB layers, leading to further cost reduction, as in low-cost consumer products, such as ink-jet or multifunction printers and PDAs. EDN

REFERENCE

1 Lexmark International, SSCG technology, US patents 5,488,627, 5,631,920, 5,867,524, 5,872,807, and 6,617,103.

AUTHOR'S BIOGRAPHY

Cavit Ozdalga is director of marketing at Spectra-Linear, where he has worked for more than two years. He focuses on product-lifetime management and market and application definitions and strategies. Ozdalga has a bachelor's degree in electrical engineering from the University of California—Berkeley and enjoys reading history. You can reach him at cavit.ozdalga@spectralinear.com.

Drive LEDs Your Way

High Efficiency LED Drivers

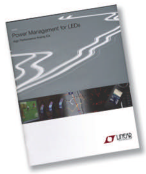
Part No.	Topology	Dimming Range	Input Voltage Range (V)	Max. Output Voltage (V)	$I_{LED (MAX)}$ (A)*	Package
LT®1618	Buck, Boost, Buck/Boost Mode	DC/PWM	1.6 to 18	36	1.00	3mm x 3mm DFN-10, MSOP-10
LT3466	Dual Boost	DC/PWM	2.7 to 24	39	0.02 x 2	3mm x 3mm DFN-10
LT3474/-1	Buck	400:1 PWM	4 to 36	9/25	1.00	TSSOP-16E
LT3475/-1	Dual Buck	3000:1 PWM	4 to 36 (40 Max.)	9/25	1.50 x 2	TSSOP-20E
LT3476	Quad Buck, Boost, Buck/Boost Mode	1000:1 PWM	2.8 to 16	36	1.00 x 4	5mm x 7mm QFN-38
LT3477	Buck, Boost, Buck/Boost Mode	DC/PWM	2.5 to 25	40	2.00	4mm x 4mm QFN-20, TSSOP-20E
LT3478/-1	Buck, Boost, Buck/Boost Mode	3000:1 PWM	2.8 to 36 (40 Max.)	40	4.00	TSSOP-16E
LT3486	Dual Boost	1000:1 PWM	2.7 to 24	35	0.10 x 2	3mm x 5mm DFN-16
LT3496	Triple Buck, Boost, Buck/Boost Mode	3000:1 PWM	3 to 30 (40 Max.)	45	0.50 x 3	4mm x 5mm QFN-28
LT3517/18	Buck, Boost, Buck/Boost Mode	5000:1 PWM	3 to 30 (40 Max.)	45	1.0/2.0	4mm x 4mm QFN-16
LT3590	Buck Mode	200:1 PWM	4.5 to 55	n/a	0.05	2mm x 2mm DFN-6, SC-70
LT3595	Buck Mode	3000:1 PWM	4.5 to 45	n/a	0.05 x 16	5mm x 9mm QFN-56
LT3755/56	Buck, Boost, Buck/Boost Mode	3000:1 PWM	4.5 to 40/6 to 100	60/100	Ext. FET	3mm x 3mm QFN-16, MSOP-16E
LTC®3783	Buck, Boost, Buck/Boost Mode	3000:1 PWM	3 to 36	40	Ext. FET	4mm x 5mm DFN-16, TSSOP-16E

*Actual output current will depend on V_{IN}, V_{OUT} and topology.

Info & Free Samples

www.linear.com/LEDdrivers

1-800-4-LINEAR



Free Power Management for LEDs Brochure

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LINEAR TECHNOLOGY

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READERS SOLVE DESIGN PROBLEMS

High-voltage, high-frequency amplifier drives piezoelectric PVDF transducer

Enrique Vargas, Sergio Toral, Vicente González, and Raúl Gregor,
Universidad Católica Nuestra Señora de la Asunción,
Itapúa Antequera, Paraguay

Piezoelectric transducers find use in NDE (nondestructive-evaluation) applications. The PVDF (polyvinylidene-fluoride) transducer has many advantages, including a wide bandwidth and high sensitivity. These transducers require high-voltage and wide-bandwidth amplifiers. The basis of the circuit in **Figure 1** is an earlier Design Idea (**Reference 1**). The operation of the circuits is basically the same, but this one can drive a 2.3-nF capacitive load at frequencies as high as 500 kHz.

In this circuit, an LM7171 op amp from National Semiconductor (www.national.com) replaces the LF411, also from National Semiconductor, of the earlier design. The LM7171 op amp has a unity-gain bandwidth of 200 MHz. To further improve the bandwidth, this design's mirror circuit uses lower-value resistors to increase the current in the transistors, thus increasing the bias current and the power dissipation of Q_3 and Q_4. To improve thermal stability, this design adds resistors R_{16} and R_{17}, and, to increase the current to drive the transducer's capacitive load, this design adds a current driver to the circuit's output. V_{CC} and V_{EE} are 15 and −15V, respectively, and V_{H+} and V_{H-} are a maximum of 150 and −150V, respectively. EDN

DIs Inside

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▶To see all of *EDN*'s Design Ideas visit www.edn.com/designideas.

REFERENCE

1 Duggal, Bipin, "High-voltage amplifier drives piezo tubes," *EDN*, Dec 7, 2004, pg 100, www.edn.com/article/CA484492.

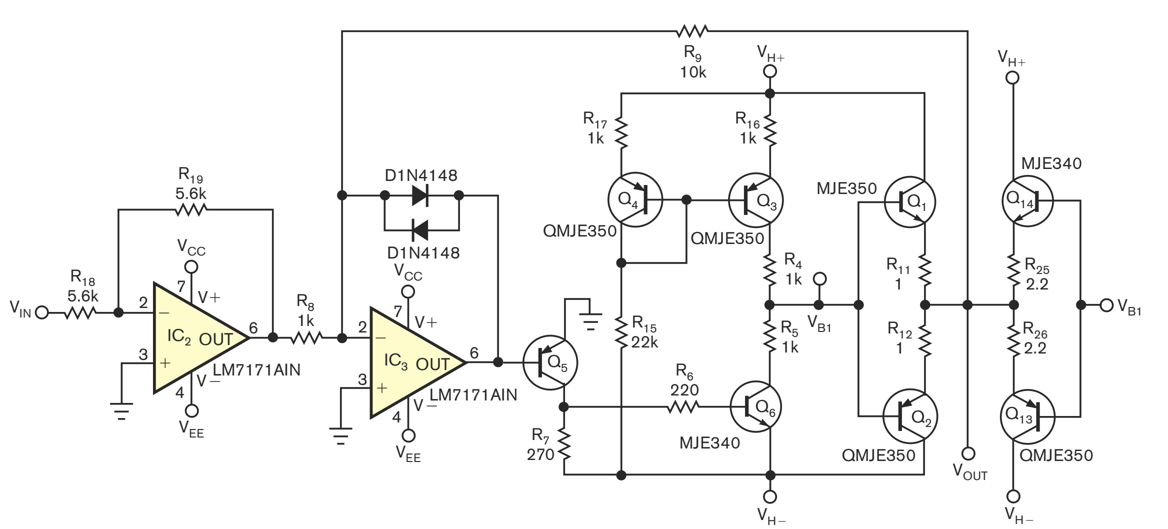

Figure 1 This high-frequency, high-voltage amplifier can drive the capacitive load from a PVDF (polyvinylidene-fluoride) piezoelectric transducer.

Microcontroller detects pulses

Abel Raynus, Armatron International, Malden, MA

While recently designing an automatic test station employing a microcontroller, I faced a nonstandard task: Detect the presence or the absence of output pulses in the DUT (device under test). You might think this task is easy to accomplish by connecting an LED to the DUT output. The blinking LED provides evidence of the pulse's presence. That approach would work if that test were the only one you needed to perform. In this station, however, the pulse test is just one of more than a dozen tests and measurements. The test station should display the final result—pass or fail—only after completing all the tests. So, it should represent the result of each test in binary format—that is, yes for pass or no for fail. This Design Idea describes a simple way of solving this problem.

The pulses for detection enter the $\overline{IRQ}$ (interrupt-request) pin of the Freescale (www.freescale.com) MC68HRC908JK1 microcontroller (**Figure 1**). Each pulse period is 500 msec, causing an external interrupt. At least three interrupts should occur within 2 seconds. The program waits for 2 seconds, and, if no external interrupts occur during that time, it declares that the pulse test has failed. The red LED on the PB1 pin then switches on, and the test stops. Otherwise, after three interrupts, the program starts the next test. To evaluate the pulse test separately from the rest of the tests, this demo program ends in an indefinite loop instead of starting the next test. When the green LED on the PB0 pin lights up, it indicates that the pulse test has successfully completed. The LEDs work with built-in current-limiting resistors, such as W934GD5V and W934ID5V devices from Kingbright (www.kingbright.com).

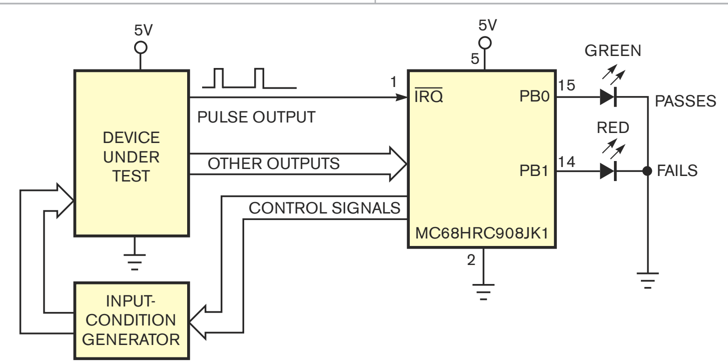

Figure 1 This 8-bit, low-end microcontroller detects pulses from LEDs, yielding a simple tester.

This design uses the low-end, 8-bit MC68HRC908JK1 microcontroller because of its low cost and ability to have 10 8-bit ADC channels. You can find **Listing 1**, the firmware-assembly code for the device, at the Web version of this Design Idea at www.edn.com/080724di1. You calculate the time delay for the oscillation frequency at approximately 4 MHz, which a 20-kΩ resistor and a 10-pF capacitor determine. This approach is applicable to any type of microcontroller because it uses standard assembly instructions. You need to recalculate the time delay only in case of different oscillation frequencies. **EDN**

Sample-and-hold amplifier holds the difference of two inputs

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

You can fulfill a requirement for sampling the difference of two signals in two classic ways. You can subtract the two input signals with an instrumentation amplifier whose output connects to an input of a classic sample-and-hold amplifier. Despite the positive feature of needing no external resistors for a gain-of-one differencing instrumentation amplifier, this approach suffers from high relative output distortion when the inputs are of the same polarity and close in magnitude. In such a case, the difference of two input signals is close to 0V, and the amplifier is therefore more vulnerable to residual dynamic imperfections of the sample-and-hold amp. The other approach is to separately sample the two input voltages in two sample-and-hold amps and subtract the outputs of these amps in an instrumentation amp. Here, the relative error of output signal with similar input waveforms is lower than in the first approach.

If you like all-in-one solutions, you can use the circuit configuration in **Figure 1**. This circuit simultaneously tracks both input voltages, V_{INA} and V_{INB}, at an active-high level of the internal logic-control signal, which enables the A_1, B_1, and A_2 voltage followers. V_{INA} thus appears on capacitor C_2, which is ground-referenced. Capacitor C_1, which is temporarily grounded at its upper node, Pin 9 of IC_1, tracks the V_{INB} voltage. After a settling interval when all of the internal logic-control signals go inactive low, the Q_{SB} logic-control signal goes high. The voltage of $V_{C2}(TS)=V_{INA}(TS)$ shifts the potential at the lower node of capacitor C_1 because of the enabled B_3 follower. Upon the sample command, Q_S is high, and the upper node of C_1 is grounded within the tracking interval. Storage capacitor C_3 therefore charges through the B_2 follower to a voltage of $V_{C2}(TS)-V_{C1}(TS)=V_{INA}(TS)-V_{INB}(TS)$. The A_3 follower serves as an impedance converter.

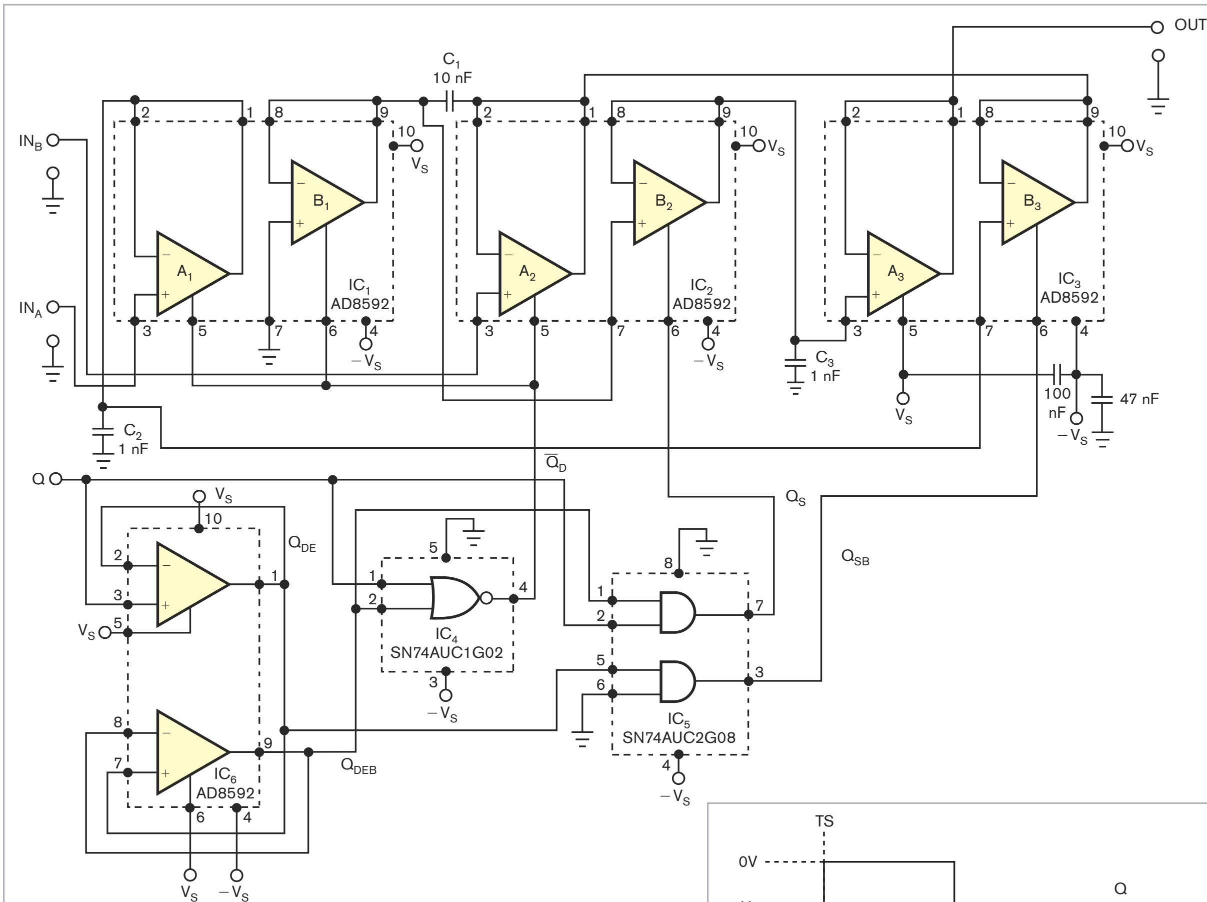

Figure 1 The basis for the operation of this circuit is the simultaneous tracking of the V_{INA} and V_{INB} input voltages on capacitors C_1 and C_2 and a stacking of these capacitors within the sample interval on capacitor C_3.

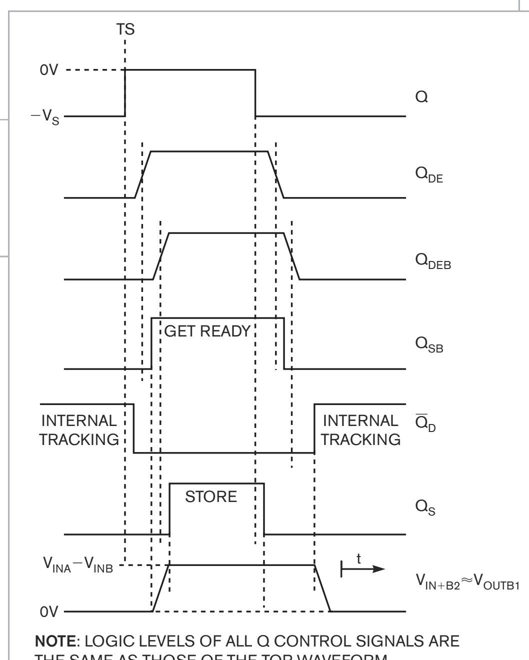

Figure 2 The bottom waveform shows that, at the upper node of capacitor C_1, 0V appears within the tracking interval, and it rises to the value of a difference between both input voltages within the get-ready interval when Q_{SB} is high. The difference of input voltages of $V_{INA}(TS)-V_{INB}(TS)$ resides within the store interval when Q_S is high.

The voltage gains of both the A and the B channels are slightly lower than ideal. This slight gain decrease has approximately the same value for both channels: $\delta_{GAINA}=\delta_{GAINB}\sim(C_{OUTB1}/C_1)$. The equality of gain decrements on both channels stems from the fact that the upper node of the storage capacitor, C_1, connects at the instant that Q_{SB} goes high to the output capacitor, C_{OUTB1}, of the disabled follower, B_1. Follower B_1 always discharges to 0V within the tracking interval without regard to the voltages at the A and B inputs. For Analog Devices' (www.analog.com) AD8592 op amps, the output capacitance, C_{OUT}, in the disabled state is approximately 26.2 pF.

Note, however, that if V_{INA} and V_{INB} are of opposite polarity and of equal magnitude, almost reaching the value of $V_S/2$, the output voltage approaches either the positive- or the negative-supply rail. In this case, the relative output error is about twice that given in the previous **equation**. The op amps' capacitance rises as the output voltage approaches any of the supply rails, reaching the value of 55 pF. This increasing output capacitance arises from one of the complementary power transistors in the AD8592's output stage as its drain-to-source voltage approaches 0V at the output voltage close to the positive-supply rail. The increasing drain-to-source capacitance with decreasing drain-to-source voltage is an inherent property of MOSFET transistors. The same situation holds true for the bottom power transistor of the AD8592's output stage, when the output voltage approaches the negative-supply rail.

The turn-on time of the AD8592 is much longer than the turn-off time. Although the device's data sheet does not directly specify these times, you can see from the internal structure of the IC that the on/off control enters almost all of the IC's stages (**Reference 1**). Thus, turn-off is fast because the turn-off of the output stage occurs without regard for the states of the preceding stages.

Within one period of operation of the circuit in **Figure 1**, a sequence of two turn-ons (T_{ON}) plus four intentionally added delays (T_{DE}) determines the shortest sampling period: $T_{MIN} \sim T_{ONB3} + 4T_{DE} + T_{ONA1B1A2}$. Here, $T_{ONA1B1A2}$ is the largest from among the values of turn-on times of followers A_1, B_1, and A_2, which depend on the actual values of V_{INA} and V_{INB}. The maximum sampling frequency is then $1/2(T_{ON}+2T_{DE})$.

If you assume that the maximum turn-on time can reach the value of the overvoltage-recovery time of approximately 3 μsec and that the delay time is approximately 0.35 μsec, then it follows that the maximum sampling frequency is approximately 135 kHz. The duty-factor of the external logic-control signal, Q, for sampling frequencies near the value of the maximum sampling frequency should be about 0.5 (**Figure 2**).EDN

REFERENCE

1 "AD8592-Dual, CMOS Single Supply Rail-to-Rail Input/Output Operational Amplifier," Analog Devices Inc, 1999, www.analog.com/zh/prod/0,,759_786_AD8592,00.html.

Precision capacitive-sensor interface suits miniature instruments

Jiaqi Shen and Xiaoshu Cai,
University of Shanghai for Science and Technology, Shanghai, China

In some applications of capacitive sensors, the instrument's front end must be small enough to fit into a narrow space. **Figure 1** shows a precision capacitive-sensor interface for such use. The square-wave output from a low-voltage 555 timer, IC_1, constantly triggers the precision one-shot, IC_2, to produce quasistable outputs for time periods T_1 and T_2, which are proportional to external timing capacitance: $T_1 = KR_0(C_S + C_0)$, and $T_2 = KR_0C_S$, where K is the multiplier factor. K is nearly independent of the external timing capacitance when that capacitance is more than 100 pF (**Reference 1**). So, a 150-pF capacitor, C_0, in shunt with the capacitive sensor, C_S, supplies an offset so that operation of the one-shot remains within a linear range even if the value of C_S is less than 100 pF.

To achieve good measurement accuracy, connect a reference channel with a fixed 150-pF capacitor. This method cancels the effects of both stray capacitance and transition time. A single 3.3V supply powers this interface circuit. The circuit's compact design permits flexibility, and you can easily

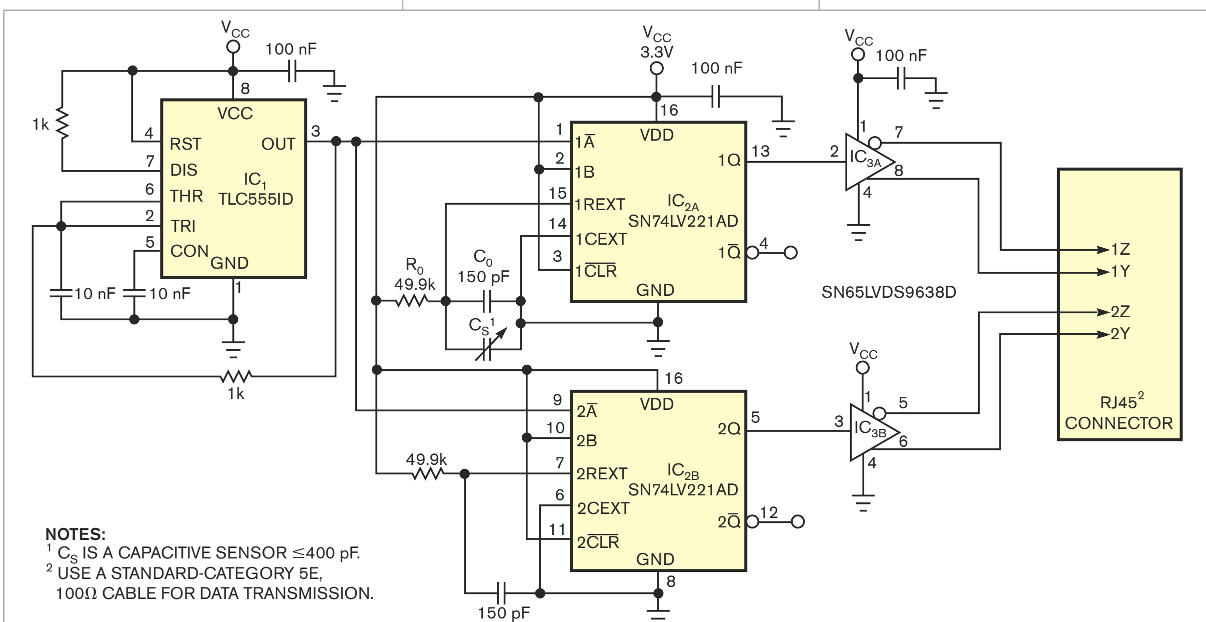

Figure 1 This compact capacitive-sensor-interface-circuit design permits great flexibility; you can easily integrate it into a miniature sensor head near the measurement point.

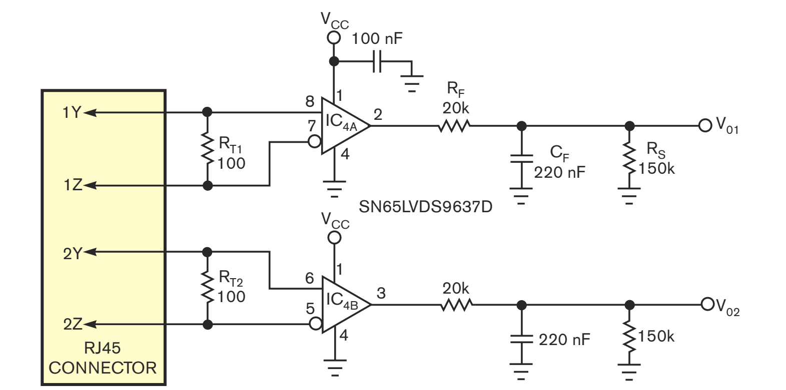

Figure 2 At the terminal, IC_4 converts the signals it receives from the interface to LVTTL levels and then feeds them to a set of passive filters.

integrate the circuit into a miniature sensor head near the measuring point. IC_3 converts the outputs to LVDS (low-voltage-differential-signaling) levels and then transmits these outputs using a standard Category 5e cable to the terminal, which may be some distance away. As long as the cable is shorter than 10m, the transmission bandwidth is adequate for ensuring acceptable measurement accuracy within several picofarads to hundreds of picofarads (**Reference 2**). In **Figure 2**, the terminal at IC_4 converts the signals it receives from the interface to LVTTL (low-voltage-transistor-to-transistor-logic) levels and then feeds them to a set of passive filters. Each dc output is proportional to the signal's duty cycle:

$$V_{O1} = V_H \times \frac{T_1}{T_P} \times \frac{R_s}{R_f + R_s},$$

and

$$V_{O2} = V_H \times \frac{T_2}{T_P} \times \frac{R_s}{R_f + R_s},$$

where V_H is the high-level output voltage of IC_4 and T_P is IC_1's oscillation period. By digitizing the two outputs, you can obtain a reading proportional to the sensor's capacitance, $V_{O1} - V_{O2}$. Be sure that $T_1 < T_P$,—that is, $C_S < T_P/(K \times R_0) - C_0$; otherwise, the final output will be erroneous. For the sake of a wide measurement range, keep T_P as long as the target application permits. **EDN**

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1 "SN54LV221A, SN74LV221A: Dual Monostable Multivibrators With Schmitt-Trigger Inputs," Texas Instruments, April 2005, http://focus.ti.com/lit/ds/symlink/sn74lv221a.pdf.

2 High-performance linear products technical staff, *LVDS Application and Data Handbook*, Texas Instruments, November 2002, http://focus.ti.com/lit/ug/slld009/slld009.pdf.

BY SUZANNE DEFFREE

supplychain

LINKING DESIGN AND RESOURCES

Online business booming for catalog distributors

Online sales may still be a small percentage of total distribution sales, but it's a growing opportunity, especially for catalog distributors.

According to Mark Larson, president of Digi-Key Corp (www.digikey.com), Internet sales accounted for 62% of the distributor's total sales in 2007, compared with 54% in 2006. Larson expects that Digi-Key will derive 70% of its sales through the Internet in 2008.

"As a distributor with a catalog background, sales via our Web site seemed like a natural extension of what we were already doing—a better way of reaching customers," he says.

According to *EDN*'s May Top 25 North American Electronic Component Distributors ranking, total 2007 sales at Digi-Key were $941.1 million. The company showed a 14% increase over its reported 2006 revenue.

The story is a similar one at Newark (www.newark.com), part of the global Premier Farnell Group. "While Newark is a multichannel distributor with branches, call centers, and an outside-sales team, we're quickly emerging as a dynamic Web business," says Barry Litwin (**photo**, left), senior vice president of marketing. "As such, one of our target goals for the decade is to more than double our Web sales, so that 50 to 70% of our entire sales come through that channel. Our market research suggests that both electronic-design engineers and buyers prefer to use the Web to find, quote, and order online."

Newark's total sales in 2007 were $627.5 million, according to *EDN*'s Top 25 North American Electronic Component Distributors ranking. The company showed a 3% year-over-year gain in its reported 2007 revenue.

GREEN UPDATE

CITY COUNCIL OVERRIDES MAYOR'S EFFORTS TO TRASH NEW YORK E-WASTE BILL

The Big Apple may soon put the burden on electronics manufacturers when it comes to the recovery of e-waste (electronics waste).

The New York City Council (www.council.nyc.gov) overrode Mayor Michael Bloomberg's (**photo**, right) spring veto of a bill that requires electronics manufacturers to take back a minimum of 25% of what they sell by July 1, 2012. That percentage will rise to 65% in 2018.

Introductory Bill No. 729 would amend New York's Electronic Equipment Collection Recycling and Reuse Act and, in Bloomberg's view, disproportionately burdens electronics manufacturers instead of wholesalers that sell directly to the public.

AEA (www.aeanet.org, formerly the American Electronics Association), one of the nation's largest high-tech trade groups, opposes collection standards at any level and supports Bloomberg's veto.

"AEA does not support the use of performance measurements, particularly those that enforce strict penalties regardless of manufacturer compliance and success with the particular recycling program," says Justin Wright, AEA's Northeastern policy director. "Additionally, manufacturers cannot compel or require private citizens to turn in their property at all, let alone according to some statutory schedule."

The Council overrode Bloomberg's veto, but he is not expected to implement the standards. To comment on the bill, go to www.edn.com/blog/690000269/post/1690026569.html.

OUTLOOK

MID-IC DEMAND TO CLIMB

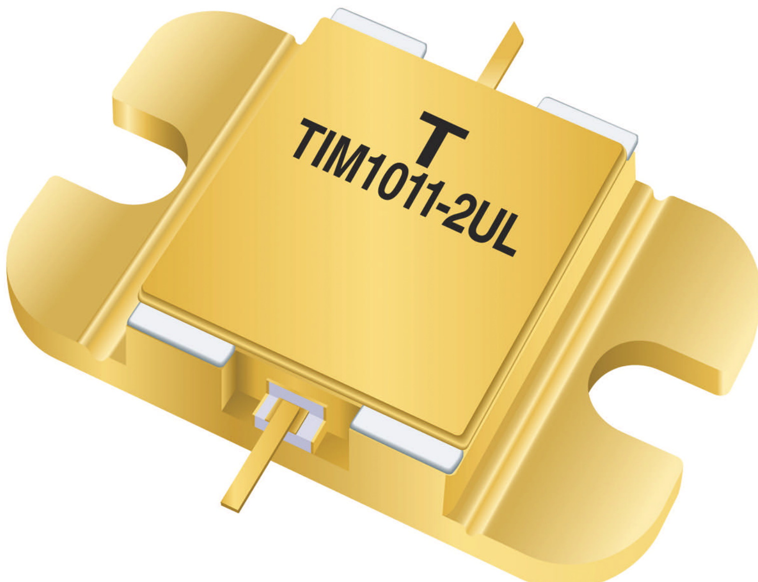
Analysts expect global shipments of MIDs (mobile Internet devices) to skyrocket in the next four years, as will demand for the ICs in the small devices. Research from Forward Concepts (www.fwdconcepts.com) predicts that MID shipments will grow from 305,000 units in 2008 to almost 40 million in 2012, reaching $12 billion in revenue. Analysts forecast IC revenue from MIDs will grow from $29 million in 2008 to $2.6 billion in 2012.

According to Forward Concepts, Texas Instruments (www.ti.com) is one of the two best-positioned non-x86-semiconductor vendors for supplying stand-alone application processors for MIDs. The company attributes that position to TI's mature and proven OMAP (Open Multimedia Application Platform) application-processor family and its top market-share position in the stand-alone-smartphone-application-processor market.

Qualcomm (www.qualcomm.com) is the other best-positioned non-x86-semiconductor vendor, according to Forward Concepts, which points to Qualcomm's market-leading 3G wireless products for the MID market. Intel (www.intel.com), which has been pushing MIDs as part of its Atom-processor-marketing strategy, has a much better shot at UMPCs (ultramobile personal computers), Forward Concepts says.

productroundup

DISCRETE SEMICONDUCTORS



Power-added amplifiers claim improved power efficiency

Aiming at microwave-digital radios and block-up converters, the X-band GaAs FETs support point-to-point and point-to-multipoint terrestrial communications. Operating over a 10.7- to 11.7-GHz range, the TIM1011-2UL and the TIM1011-8UL provide 36 and 39% power-added efficiency, respectively. The TIM1011-2UL has a typical output power of 2W or 33.5 dBm at a 1-dB-gain-compression point. The TIM1011-8UL has a typical output power of 8W or 39.5 dBm at a 1-dB-gain-compression point and 9-dB typical linear gain. Targeting satellite applications, the TIM5964-30UL and the TIM7785-30UL 30W C-band power amplifiers operate over 5.9- to 6.4- and 7.7- to 8.5-GHz frequency ranges, respectively. These devices suit use in block-up-converter applications for small-aperture terminals and solid-state power amplifiers. The TIM5964-30UL has a typical output power of 45 dBm at 1-dB-gain-compression and a 10-dB typical gain. The TIM7785-30UL features a typical output power of 45 dBm at a 1-dB gain-compression point and a 9-dB typical gain. The TIM5964-30UL and the TIM7785-30UL amplifiers provide 41 and 39% power efficiency, respectively. The TIM1011-2UL and the TIM1011-8UL devices cost $217.50 and $405, respectively; the TIM5964-30UL and the TIM7785-30UL amplifiers cost $450 and $742.50, respectively.

Toshiba America Electronic Components, www.toshiba.com

30V DirectFET MOSFETs provide footprint flexibility

Providing 25A-per-phase operation, the IRF672X family of 30V DirectFET MOSFETs target synchronous-buck-converter designs for notebook computers, server-processor power, graphics, and memory-voltage-regulator applications. Combining the vendor's 30V HEXFET power-MOSFET silicon with DirectFET-packaging technology allows a 0.7-mm profile and a 40% reduction in footprint compared with standard SO-8 devices. The IRF6724M, IRF6725M, IRF6726M, and IRF6727M feature a 1.5- to 1.2-mV typical on-resistance, suiting high-current synchronous MOSFETs. An 11-nC typical gate charge and a 3.7- to 4.3-nC typical gate-to-drain charge make the devices suitable for control MOSFETs. Prices for the IRF6724M, IRF6725M, IRF6726M, and IRF6727M range from $1.10 to $1.50 (1000). The IRF6721S, IRF6722S, and IRF6722M are available in SQ, ST, and MP footprints, and prices range from 60 to 75 cents (10,000).

International Rectifier, www.irf.com

SCR electronic shunt aims at high-reliability-LED-lighting applications

The NUD4700 SCR electronic shunt provides a current bypass for a single LED connecting to an open circuit. Targeting high-reliability-LED-lighting applications, such as headlights, lighthouses, bridges, aircraft, and runways, the shunt protects LEDs from transient and surge conditions. Features include a 1V typical on-state voltage and a 250-μA off-state current, preventing a string of LEDs from going off when one LED fails. Aiming at 1W LEDs—nominally, 3V at 350 mA—the device suits applications requiring circuit continuity. The NUD4700 electronic shunt costs 10 cents (3000).

On Semiconductor, www.onsemi.com

ESBT power switch aims at one- to three-phase applications

The STC03DE220HV ESBT (emitter-switched-bipolar-transistor) power switch targets auxiliary switched-mode power supplies for single- and three-phase applications. Rat-

DESIGN NOTES

Dual 8A DC/DC µModule Regulator Is Easily Paralleled for 16A

Design Note 446

Eddie Beville and Alan Chern

Two Independent 8A Regulator Systems in a Single Package

The LTM®4616 is a dual input, dual output DC/DC µModule™ regulator in a 15mm × 15mm × 2.8mm LGA surface mount package. Only a few external components are needed since the switching controller, MOSFETs, inductor and other support components are integrated within the tiny package.

Both regulators feature an input supply voltage range of 2.375V to 5.5V and an adjustable output voltage range of 0.6V to 5V with up to 8A of continuous output current (10A peak). For higher output current designs, the LTM4616 can operate in a 2-phase parallel mode allowing the part to deliver a total output current of 16A. The default switching frequency is set to 1.5MHz, but can be adjusted to either 1MHz or 2MHz via the PLLLPF pins. Moreover, CLKIN can be externally synchronized from 750kHz to 2.25MHz. The device supports output voltage tracking for supply rail sequencing. Safety features include protection against short circuit, overvoltage and thermal shutdown conditions.

Simple and Efficient

The LTM4616 can be used as completely independent dual switching regulators with different inputs and outputs or paralleled to provide a single output. Figure 1 shows a typical design for a 5V common input and two independent outputs, 1.8V and 1.2V. Figure 2 shows the efficiency of the circuit at both 5V and 3.3V inputs.

Few external components are needed since the integrated output capacitors can accommodate load steps to the full 8A. Each output voltage is set by a single set resistor from FB1 (or FB2) to GND. In parallel operation, the FB pins can be tied together with a single resistor for adjustable output voltage.

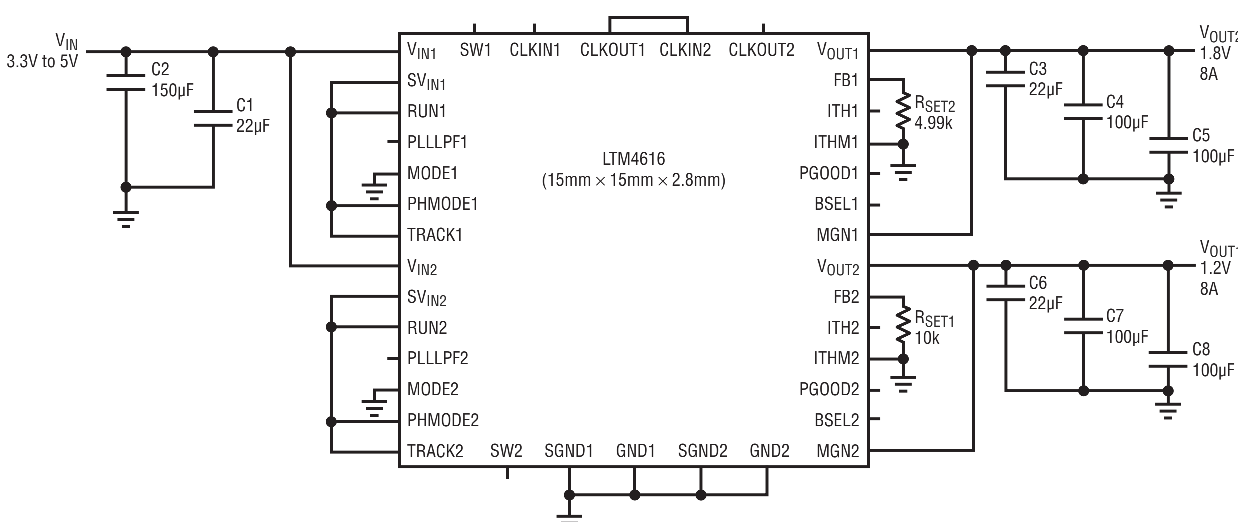


Figure 1. Dual Output LTM4616 for a Single 3.3V to 5V Input, Independent 1.8V and 1.2V Outputs at 8A Each

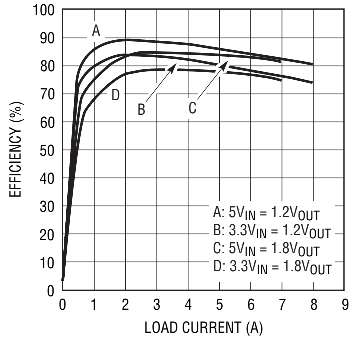


Figure 2. LTM4616 Efficiency: Dual Output

Parallel Operation for Increased Output Current

You can double the maximum output current to 16A by running the two outputs in parallel as shown in Figure 3. Note that the FB pins share a single voltage-set feedback resistor that is half the value of the feedback resistor in the usual two output configuration. This is because the internal 10kΩ top feedback resistors are in parallel with one another, making the top value 5kΩ.

It is preferred to connect CLKOUT1 to CLKIN2 when operating from a single input voltage. This minimizes the input voltage ripple by running the two regulators out of phase with each other. If more than 16A output current is required, then multiple LTM4616 regulators can be configured for multiphase operation with up to 12 phases via the PHMODE pin. Figure 4 shows the expected efficiency of the parallel system at 5V and 3.3V inputs to 1.8V output. Note that the two regulators drive equal output current even during soft-start, as shown in Figure 5.

Conclusion

Whether you require a single 16A high current output or dual 8A outputs with sequencing, the LTM4616 provides a simple and efficient solution.

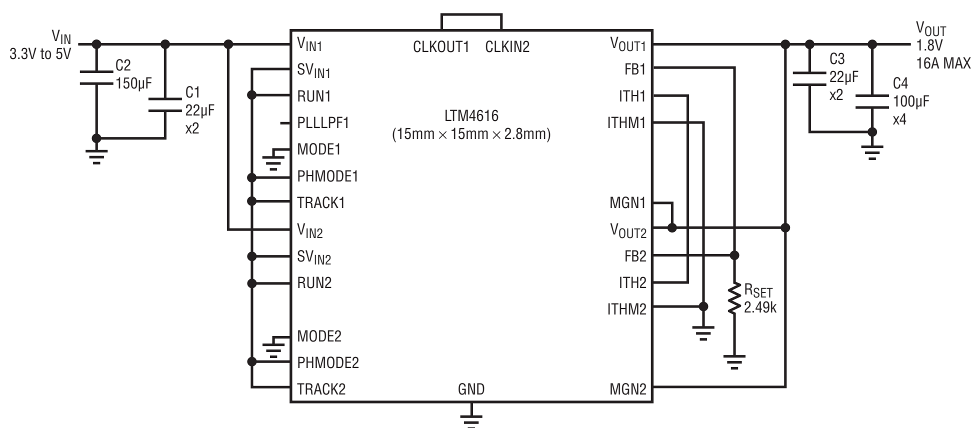


Figure 3. LTM4616 with 16A Parallel Operation

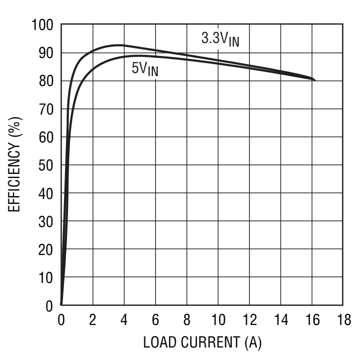


Figure 4. LTM4616 Efficiency: Single 1.8V Output

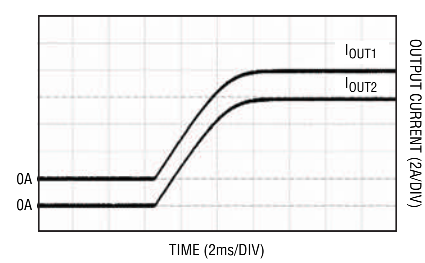


Figure 5. Balanced Current Sharing for Even Heat Dissipation [$5V_{IN}$ to $1.8V_{OUT}$ at 16A]

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productroundup

DISCRETE SEMICONDUCTORS

ed for a 2200V breakdown voltage, the switch allows a single-switch flyback topology in universal-input converters operating from 90 to 690V ac. Features include a 0.33V on-resistance from the collector source, a 150-kHz maximum switching frequency, and a 3A maximum rated current. An enhanced TO247-4L package provides an 8.9-mm creepage distance, exceedintg IEC664-1 specifications at the 2200V maximum working voltage. The STC03DE220HV costs $3.50 (1000).

STMicroelectronics, www.st.com

Half-bridge IGBT module series provides 75 to 200A current ratings

The half-bridge IGBT series includes eight 600 and 1200V modules with 75 to 200A current ratings. The series features three IGBT technologies, suiting a variety of applications. The GA100TS60SFPbF and the GA200HS60S1PbF provide standard punch-through IGBT technology; the GA200TS60UPbF, the GA75TS120-UPbF, and the GA100TS120UPbF use Generation 4 technology for tighter parameter distribution and improved efficiency. The GB100TS60NPbF, the GB150TS60NPbF, and the GB200TS-60NPbF modules offer Generation 5 non-punch-through technology, allowing 10-µsec short-circuit capabilities. The GA100TS60SFPbF and GA-200HS60S1PbF standard-speed devices suit hard switching at 1-kHz operating frequencies. The other six ultrafast modules in the family come with Hex-Fred ultrasoft-recovery antiparallel diodes aiming at bridge configurations. The ultrafast devices target 8- to 60-kHz operating frequencies in hard-switching mode and 200 kHz in resonant mode. The modules are available in the Int-A-Pak package, and prices range from $42 to $72.71.

Vishay Intertechnology, www.vishay.com

N-channel MOSFETs provide improved power density

The OptiMOS 3 N-channel MOSFETs claim as much as 50% better power density than standard-transistor-outline packages. Targeting synchronous-rectification applications in server-switch-mode power supplies, the 40, 60, and 80V SuperSO8 devices deliver D^2-Pak on-resistance values of 1.8, 2.8, and 4.7 mΩ, respectively, with a 20% reduction in space requirement. The packages feature 0.5-nH inductance, reducing ringing under switching conditions. The 1-mm-high MOSFETs have a 16K/W junction-to-topside thermal resistance, making them suitable for use in devices implementing topside cooling in embedded systems or PCB-based modules for vertical placement in 3-D integrated systems. The devices are available in SuperSO8 and Shrink SuperSO8 packages; the 60V SuperSO8-packaged OptiMOS 3 costs 99 cents.

Infineon Technologies AG, www.infineon.com

COMPUTERS AND PERIPHERALS

High-performance hard drive has 10,000-rpm spin rate

The VelociRaptor SATA hard drive has twice the capacity, better performance, and higher overall speed than the vendor's Raptor hard-drive series. The drive uses 300 Gbytes of high-performance storage with a 10,000-rpm spin rate. The device includes a 2.5-in. HDA (head-disk as-

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productroundup

COMPUTERS AND PERIPHERALS

sembly) but comes inside the vendor's IcePack, allowing the device to fit into 3.5-in. frames and maintaining proper cooling at maximum and sustained performances. Available in Alienware's high-performance ALX gaming desktop, the VelociRaptor WD3000GLFS costs $299.99.

Western Digital, www.wdc.com

SATA-hard-disk-drive adapter aims at notebook computers

Targeting notebook computers, the Dual CF SATA hard-disk-drive adapter suits the devices for use as solid-state compact-flash systems. The CF I and CF II cards allow configuration as RAID 1, RAID 0, or combined as a large CF drive. The CF SATA hard-disk-drive adapter costs $79.99.

Addonics Technologies, www.addonics.com

Graphics card provides dual-stream high-definition video

Based on the low-profile PCIe Gen 2 graphics-card specifications, the S3 Graphics Chrome 440 GTX provides PCs with dual-stream picture-in-picture 1080p Blu-Ray-disc playback. The device uses a 64-bit, DDR3 memory-bus interface, and allows HDMI connections with audio, dual-link DVI, and an optional CRT connector. The S3 Graphics Chrome 440 GTX costs $69.

S3 Graphics, www.s3graphics.com

USB drive features AES encryption

FIPS-certified by the US government, the DTBB (DataTraveler BlackBox) USB drive offers 256-bit hardware-based AES encryption. The drive automatically locks up after 10 unsuccessful password attempts. The device provides 24-Mbyte/sec data-transfer rates for reads and 20 Mbytes/sec for writes. A titanium-coated stainless-steel casing has waterproof certification as deep as 4 ft. Measuring 3.06×0.9×0.47 in., the 2-, 4-, and 8-Gbyte DTBB models cost $165, $242, and $424, respectively.

Kingston Technology, www.kingston.com

Solid-state drive has a 1-in. form factor

Providing support for native SATA and PATA interfaces, the 1-in. Mach4 solid-state drive sustains sequential 90-Mbyte/sec read speeds and 55-Mbyte/sec write speeds. The drive uses a built-in 8-bit ECC engine and power-down data protection. Security features include AES encryption in the hardware, write-protect, and data-purge applications. Providing an industrial and commercial operating-temperature range, the 8-Gbyte Mach-4 solid-state drive costs $45.

Stec, www.stec-inc.com

Hard-drive-upgrade kit has a dual SATA/PATA interface

The EZ Upgrade notebook hard-drive-upgrade kit uses a dual SATA/PATA interface. Features include a high-speed 2.0 hard-drive enclosure with USB 1.1 compatibility, a USB cable, and the vendor's upgrade suite. The upgrade suite includes the vendor's EZ Gig II cloning and imaging software for Windows and Shirt Pocket's SuperDuper! for Macs. The notebook hard-drive-upgrade kit costs $49.

Apricorn, www.apricorn.com

productroundup

INTEGRATED CIRCUITS

Touchscreen-controller IC includes low-power features

The four-wire STMPE811 resistive-touchscreen-controller IC functions autonomously, reducing demands on the host processor. Built-in features include an internal 12-bit ADC for high resolution, as well as 128×32-bit FIFO-data buffers, allowing smooth position tracking. The IC provides a less-than-1-mA active current, a 1-µA idle current, and a 150-nA hibernation mode. Available in a 3×3-mm QFN-16 package, the STMPE811 touchscreen-controller IC costs 95 cents (10,000).

STMicroelectronics, www.st.com

Image-processing devices provide standard- and high-definition support

Based on the vendor's EMMA (enhanced-multimedia-architecture) platform, the EMMA3SL/SD and the EMMA3SL/HD image-processing devices support the H.264 video-compression standard. The EMMA3SL/SD suits standard-definition-video broadcasts, and the EMMA3SL/HD supports high-definition broadcasts. The devices include a built-in EHCI (enhanced-host-controller-interface)-compliant USB 2.0 host controller and an IEEE 802.3/3u/802.3x-compliant Ethernet MAC. The EMMA2SL/HD system on chip provides a built-in HDMI-compliant interface. The EMMA3SL/SD and the EMMA3SL/HD image-processing devices cost $40 and $50, respectively.

NEC Electronics, www.am.necel.com

Inertial sensor targets vehicle-mounted antennas and cameras

Adding to the vendor's iSensor intelligent-sensor family, the six-degree-of-freedom ADIS16365 IMU (inertial-measurement-unit) sensor suits industrial-vehicle-navigation systems and platform-stability applications, such as vehicle-mounted antennas and cameras. The IMU claims a 20% power-consumption reduction, a 50% improved bias stability, and an improvement in start-up times over competitive units. Features include automatic sensor-point-of-reference realignment, digital-range scaling, dynamic environmental compensation, autonomous self-test, and embedded-sensor-condition monitoring. Backward-compatible with other iSensor six-degree-of-freedom sensors, the device also provides evaluation-board support. Additional features include a 17g dynamic-range accelerometer, a programmable SPI port, and a −40 to +105°C operating-temperature range. The factory-calibrated and programmable IMU combines three gyroscopes and three accelerometers and provides a 0.05°/sec/g dynamic-linear-acceleration-compensation factor. Available in a 23×23×23-mm module, the ADIS16365 costs $375 (1000).

Analog Devices, www.analog.com

H.264 codecs support QVGA to HD resolutions

The QL303 and QL305 full HD (high-definition) H.264 codecs support baseline, main, and high profiles of the H.264 standard for resolutions ranging from 320×240-pixel QVGA to 1920×1080-pixel HD. The codecs provide full HD H.264 encoding using less than 275 nW of power. Features include an on-chip DSP; a JPEG compression/decompression engine allowing simultaneous still-frame processing; and an ARM core for audio/visual synchronization, bit-stream packetization, and peripheral-interface management. The QL305 also provides additional peripheral interfaces, suiting communication and computing platforms. The QL303 and QL305 HD codecs cost $20 and $24 (10,000), respectively.

Qpixel Technology, www.qpixeltech.com

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BY HUGH SHANE • MITRE

Ghost busting on the ocean floor

DANIEL VASCONCELLOS

Some years ago, I worked for a start-up that was engaged in the manufacture and operation of side-scan sonars in seafloor-mapping operations. Like any other good start-up, my company performed its development work on a shoestring budget and was successful only by dint of young engineers like me doing long hours of overtime and late-night debugging sessions.

Although my primary responsibility was the development of digital-signal-processing hardware and software, during survey operations, I was responsible for operation and maintenance of any piece of electronic gear on the ship, including the stuff that we didn't build.

Side-scan sonars comprise two major assemblies: the "tow fish" and the surface-electronics package. The tow fish is a submersible assembly ranging in size from a torpedo to a large car, depending on the sonar operating frequency. A ship tows it at a depth that both isolates it from the effects of sea-surface-wave motion and places it below the acoustic-path-distorting thermocline. The tow fish houses a pair of port- and starboard-looking transducer arrays and their associated front-end electronics, as well as the telemetry system for sending digitized sonar returns to the surface and receiving command and control messages from the surface. The surface-electronics package consists of a real-time signal processor, which converts the sonar returns into both calibrated intensity and phase data—my specialty—and an enterprise-class computer system that produces the final backscatter images and bathymetric charts. Backscatter images are essentially monochrome maps of the reflectivity of the seafloor. Bathymetric charts are simply seafloor-contour maps.

One of the systems that we built had a chronic problem. It appeared as if data from the port and the starboard sides were somehow intermingling, causing ghost images of the port side to appear in the starboard data and vice versa. There were numerous theories about why this situation was occurring, but our development cycle never allowed us the time to get to the bottom of the problem.

I performed the tedious exercise of putting the system in a self-test mode. In this configuration, I could inject well-behaved test signals into the sonar front end and trace them through the entire system. Although we had built this capability into the system, no one until now had ever thought to use it to try to isolate the ghosting problem. Fortunately, the problem had become a persistent one, and, after a couple of hours, I isolated it to one board in the signal-processor rack. This board's function was to synchronize and demultiplex the digital-data stream that the tow fish had telemetered to the surface.

The board used mid-1980s technology and consisted mainly of dozens of 74LSxxx chips wired up as state machines, multiplexers, and the like. Oscilloscope probe in hand, suspect board on a card extender, schematics spread out on the improvised work bench, I followed the signal path from the board input into the belly of the beast. My efforts soon paid off. I discovered that an 8-bit gate that marshaled the incoming data to either the port or the starboard processing streams had a cold solder joint on its A/B control pin. So, data only sometimes made it to the right place. A quick touchup with the soldering iron fixed the problem.

Why didn't it occur sooner to us to try this test? I can't really say. In any case, our attempts to fix the problem during postprocessing amounted to sweeping the problem under the carpet. Returning to first principles saved the day. EDN

Hugh Shane is lead communications engineer at The MITRE Corp. Like Hugh, you can share your Tales from the Cube and receive $200. Contact edn.editor@reedbusiness.com.

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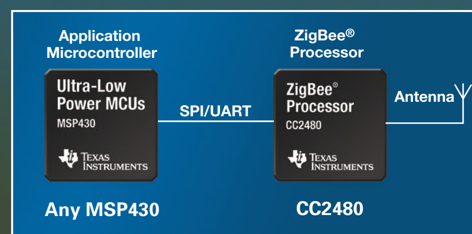

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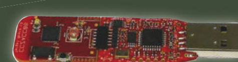

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